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Significant Enhancement of High-N_s electron mobility in Ge n-MOSFETs

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[Introduction] Recent progress of GeO_2-based MOS technology has attracted considerable attention in realization of high performance Ge CMOS beyond Si. One of the great concerns in Ge n-MOSFETs now is that electron mobility shows a substantial degradation in high-N_s region, unlike hole mobility in Ge p-MOSFETs [1]. In this work, we present the significant enhancement of high-N_s electron mobility in sub-nm EOT Ge n-MOSFETs by the combination of Y_2O_3 and low-temperature high-pressure oxidation (LT-HPO), and possible mechanisms of electron mobility enhancement is discussed.

[Experiment] pGe(100) and (111) wafers were used for MOSFETs fabrication. Several channel lengths (W/L = 25 μm/100-500 μm) were defined, and phosphorus ($1x10^{15}$ /cm^2 dose) was implanted at 70 keV through the buffer layer for source/drain formation. For gate stack formation, 1.5 nm-thick Y_2O_3 was deposited by rf-sputtering and LT-HPO was carried out at 500°C for 60 sec in 70 atm O_2 ambient. 0.7 nm-thick GeO_2 interfacial layer was grown at Ge/Y_2O_3 stack after LT-HPO. The total EOT was controlled by LT-HPO time. Al was deposited and patterned for the gate and source/drain contacts.

[Results and Discussion] **Fig. 1** shows the benchmark of the high-N_s electron mobility as a function of EOT. The high-N_s mobility of 429 cm^2/Vs in Ge n-MOSFETs with sub-nm EOT is demonstrated, which is the highest one to date among scaled EOT Si [2] and Ge MOSFETs [3-5]. It is worthy note that electron mobility in high-N_s region is significantly enhanced, compared to pure Ge/GeO_2 stack. It is worthy note that electron mobility in high-N_s region is significantly enhanced, compared to pure Ge/GeO_2 stack. In order to understand the origin of electron mobility enhancement in high-N_s region, we should consider oxidation process in Ge. **Fig. 2** shows a schematic of thermal oxidation in Ge. It is well known that viscous flow of GeO_2 occurs at relatively high temperature (> 500°C) [6]. Therefore, in Ge oxidation process, GeO_2 formation and the oxygen vacancy (V_O) formation as well as structural relaxation of GeO_2 should be considered simultaneously. In order to release the interface stress, an increase of short-range order (SRO)-roughness is likely to occur. However, low-temperature (LT) suppresses the viscous flow and HPO suppresses V_O formation thermodynamically [7]. Thus, oxidation rate is extremely low [8], resulting in a significant reduction of SRO-roughness. The intermixed Y atoms in GeO_2 can further suppress the V_O formation resulting in further reduction of roughness, and high-N_s electron mobility in Ge/GeO_x/Y_2O_3 stack with LT-HPO is dramatically enhanced.

[Reference] [1] C. H. Lee *et al.*, *IEDM*, 416, 2010. [2] T. Kawango *et al.*, *TED*, **59**, 269, 2012. [3] S. Takagi *et al.*, *IEDM*, 505, 2012. [4] W. B. Chen *et al.*, *IEDM*, 420, 2010. [5] C.-M. Lin *et al.*, *IEDM*, 509, 2012. [6] M. I. Ozhovan, *JETP*, **103**, 819, 2006. [7] S. K. Wang *et al.*, *JAP*, **108**, 054104, 2010. [8] C. H. Lee *et al.*, *APEX*, **5**, 114001, 2012.

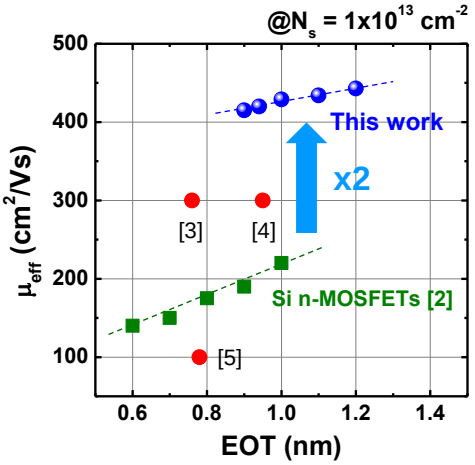

Fig. 1 High-N_s electron mobility as a function of EOT at N_s =$1x10^{13}$ cm^{-2}. The highest high-N_s mobility of 429 cm^2/Vs in Ge n-MOSFETs with sub-nm EOT is demonstrated, which is two times higher than scaled Si n-MOSFETs.

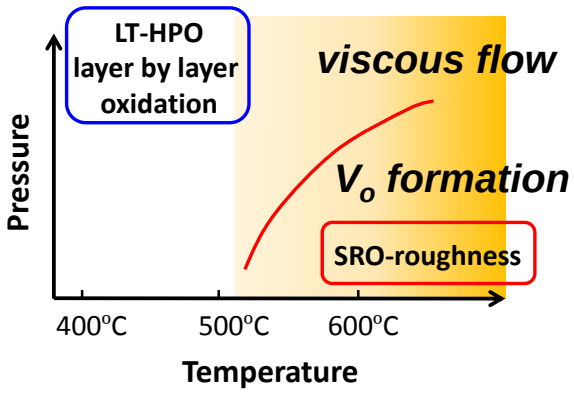

Fig. 2 Comparison of LT-HPO with conventional thermal oxidation. It is expected that viscous flow and V_O formation can relax the interface stress, while it will increase SRO-roughness. Since LT-HPO may suppress both viscous flow and V_O formation, SRO-roughness is decreased due to layer by layer oxidation with a very low oxidation rate.