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Investigation of the Substrate Orientation-Dependent on the Electrical Characteristics of HfN Gate Insulator Formed by ECR Plasma Sputtering

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1. Introduction

The high-κ gate insulator with an equivalent oxide thickness (EOT) of 0.5 nm or below is required for next generation CMOS technology. However, the formation of an interfacial layer (IL) between high-κ and Si interface is the main issues for scaling an EOT due to low dielectric constant of IL [1].

This paper presented the suppression of IL formation with EOT of 0.5 nm by using hafnium nitride (HfN) gate insulator formed by electron-cyclotron-resonance (ECR) plasma sputtering [2-3]. The influence of N_2/4.9%H_2 forming-gas (FG) annealing to the electrical characteristics and reliability of HfN gate insulator were studied. The effects of surface orientation such as Si(100) and Si(110) were investigated for three-dimensional CMOS device.

2. Experimental Procedure

First, p-Si(100) and p-Si(110) substrates were cleaned by SPM and DHF. Then HfN film (4 nm) was deposited by ECR plasma sputtering with the gas pressure of 0.20 Pa (Ar/N_2: 20/8 sccm) for 1 min [2-3]. The deposited HfN film was annealed in N_2/4.9%H_2 FG ambient with the flow rate of 1 SLM at 500°C/20 min. Finally, Aluminum electrode was deposited by evaporation through a shadow mask. The C-V and J-V characteristics of Al/HfN/p-Si MIS diodes were measured. A dual-frequency method was used to evaluate the C-V characteristics. The EOTs were extracted by using EPOQUE. The interface states density (D_{it}) was evaluated by Terman method. The time dependence dielectric breakdown (TDDB) was carried out for HfN gate insulator [4].

3. Results and Discussion

Figure 1 shows the plot between EOT and leakage current density (J_g). By using N_2/4.9%H_2 FG annealing, low EOT of 0.5 nm and 0.64 nm with the leakage current (@V_{FB} -1V) of 1.4 A/cm^2 and 1.0 A/cm^2 were obtained on Si(110) and Si(100) substrate, respectively. The V_{FB} was extracted using a capacitance from the applied voltage of -2V to 0V. The Si(110) surface has lower EOT and higher J_g compared to Si(100). The D_{it} of Si(100) and Si(110) are able to reduced down to 2.8x10^{11} and 3.0x10^{11} cm^{-2}eV^{-1}, respectively (not shown). Figure 2 shows the TDDB characteristics of Si(100) and Si(110) measured at room temperature (RT), respectively. When the voltage of -1.5V was biased, the 4 nm-thick HfN film did not breakdown until 1000 s of stress time on both Si(100) and Si(110) substrates. It should be noticed that the TDDB characteristic of Si(110) shows larger distribution compared to Si(100).

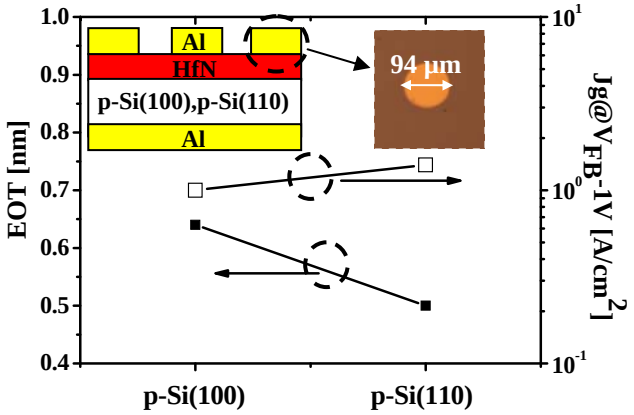

Fig. 1. EOT and J_g plots of Al/HfN/p-Si structures.

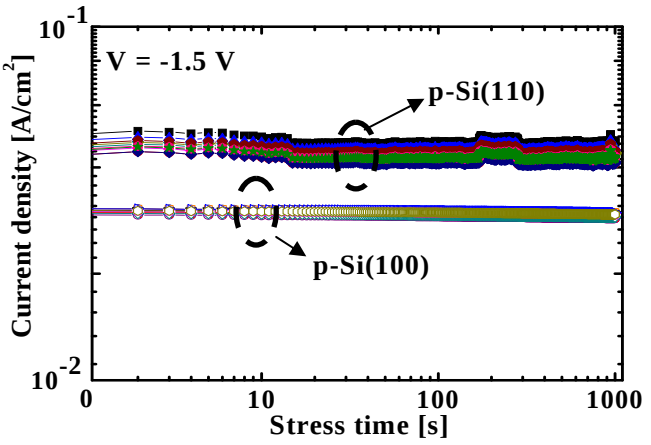

Fig. 2. TDDB characteristics measured at RT of Al/HfN/p-Si(100) and Al/HfN/p-Si(110) structures.

4. Conclusions

We investigated an effect of substrate orientation on the diode characteristic with HfN gate insulator formed by ECR plasma sputtering. The EOT of 0.5 and 0.64 nm with low J_g, low D_{it}, and without dielectric breakdown were achieved on Si(110) and Si(100), respectively.

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References

[1] Y. Morita, *et. al*., Appl. Phys. Lett., **2** (2009) 011201-1.
[2] H. Han and S. Ohmi, IEICE Electron. Express, **9** (2012) 1329.
[3] H. Han, D. Han, and S. Ohmi, Electron. Lett., **49** (2013) 500.
[4] A. Aal, IIRW final report, IEEE, (2008) 133.