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Computational Imaging Technology for Nanolithography

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Abstract

The rapid advancement of modern electronic technology is founded on Moore's Law, which stipulates an exponential increase in transistor densities, leading to more and more functionalities in an integrated circuit (IC). A critical challenge in IC manufacturing lies in the nanolithography process, where the circuit pattern on a wafer is imprinted through imaging a photomask. Because of the small feature size compared with the wavelength of the light source, image distortion is significant due to diffraction and other aberrations. Computational technology, together with the modeling of the imaging process, is now an essential process to design the source and mask patterns that can counteract the distortions and allow for the printing of small features.

1. Computational Lithography

Optical lithography has been the predominant technique for the patterning of semiconductor devices. Fundamentally, it is an imaging system, where the pattern on a photomask (or simply a mask) is transferred to the die on a wafer. For many years, optical lithography is carried out using an ArF excimer laser with a wavelength of 193nm; on the other hand, the critical dimension (CD) or feature size of the patterns continues to shrink, currently on the order of 14-22nm. Computational techniques have played a significant role since the development of model-based optical proximity correction (OPC), where the mask pattern is pre-distorted according to certain computation results to compensate for the diffraction effect in the imaging process [1,2].

Mathematically, the resolution of the lithography system is given by

$$\mathrm{CD} = k_1 \frac{\lambda}{\mathrm{NA}},$$

where λ is the wavelength of the light source and NA is the numerical aperture of the imaging system. To lower the CD, one can increase NA as far as possible, and it is normally achieved through immersing part of the lithography system in a liquid (called immersion lithography). Another possibility is to lower k_1, simply called the k_1 factor, which encapsulates all process-related effects. Computational lithography can then be viewed as a means to lower this k_1 factor.

In this talk, we highlight some of our work in computational lithography, particularly in inverse lithography and source-mask optimization.

2. Inverse Lithography and Source Mask Optimization

Inverse lithography aims to treat the mask design problem as an instance of image synthesis, an inverse problem where the mask pattern is iteratively computed based on a modeling of the lithography system [3,4]. The flexibility of this approach allows a broad design space where unintuitive mask patterns can be obtained. In addition, it is possible to add constraints for different purposes, such as robustness against process variations and mask manufacturability [5,6]. On the other hand, the highly nonlinear nature of the optimization problem in image synthesis requires heavy computation, and various optimization procedures are devised for the purpose of speeding up the calculations [7].

Lithography technology advances now permit not only a pixelated mask design but also a customizable source pattern. Their co-design is known as source-mask optimization (SMO), which is similar to inverse lithography, but promises to deliver an even broader design space at the expense of heavier computations. Considerable efforts have similarly been made on improving process robustness [8] and computational speed [9,10].

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