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Fast Computation of Computer-Generated Hologram by Using Multi-Core Processor

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1. Introduction

Electro-holography is promising for one of three-dimensional (3-D) display technologies. A hologram displayed on an electronic device such as LCD can be created by simulating propagation of the light on a computer, which is referred to as computer-generated hologram (CGH). To generate a CGH, however, it is necessary to perform a huge computation. To solve the issue, parallel computing is one of effective ways.

In this study, to accelerate CGH computation, we implemented it on various parallel computers which are multi-core CPU, GPU[1], Xeon Phi[2], and FPGA[3].

2. Theory

The complex amplitude on CGH is expressed by,

$$u_c(x_c, y_c) = \sum_{j=1}^{N} A_j \exp i\left(\frac{\pi}{\lambda z_j}((x_c - x_a)^2 + (y_c - y_a)^2)\right), \quad (1)$$

where parameters *x,y,* and *z* represent the horizontal, vertical, and depth components, while indices *c* and *j* indicate the hologram and object, respectively. *N* is the number of object points, A_j is the intensity of the object point, and λ is the wavelength of the reference light. Equation (1) is the Fresnel approximate calculation. CGH is the phase or amplitude of Eq.(1).

When the total number of pixels on CGH is M, the computational amount is proportional to MN. It becomes very huge computation. However, this computation can be accelerated by parallel computation because Eq. (1) can be calculated independently as to each pixel on CGH.

3. Specifications of Systems

CPU

We used Intel Core i7 2700K which has 4 cores (8 threads). The clock frequency is 3.5[GHz]. The CPU runs all cores using OpenMP.

GPU

We used NVIDIA Geforce GTX680 and programmed by CUDA C. The number of cores is 1,536 and the clock frequency 1.006[GHz].

Xeon Phi

Intel recently launched the Xeon Phi Coprocessor as expansion board for parallel computing. Each core on the Xeon Phi is based on the x86-architecture similar to CPU. Xeon Phi can be programmed by standard C and various libraries for parallel environment (e.g. OpenMP, MPI).

We used Xeon Phi 5110P and programmed by C and OpenMP. The number of cores is 60 (240 threads) and the clock frequency is 1.053[GHz].

FPGA

We used HORN-5 board made by ourselves in 2004, where four FPGA chips of XC2VP70 by Xilinx were mounted. We designed the circuits of Eq. (1) with pipeline method and implemented 1,280 units in the HORN-5 board. The clock frequency is 133[MHz]. In 2009, we developed the cluster system HORN-6 where 16 HORN-5 boards (20,480 units of Eq.(1) circuits) operated in parallel.

4. Result

We compared CGH computational time with Intel Core i7 2700K CPU (8 cores), NVIDIA Geforce GTX 680 GPU, Intel Xeon Phi 5110P, and our original FPGA board HORN-5. Table I shows the comparison of the computational times. Here, the CGH size is 1,920×1,080 and the number of object points is 10,000.

Table I Comparison of computational times

Processor	Computational time [ms]
Intel Core i7 2700K (CPU)	41,000
Intel Xeon Phi 5110P	2,630
NVIDIA Geforce GTX 680	196
HORN-5 (4 FPGAs)	134
HORN-6 (64 FPGAs)	11

5. Conclusions

We implemented CGH computation on various multi-core processors. Image processing is generally suitable for parallel computing. The result shows CGH calculation also accelerates depending on the number of cores.

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