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Zero Area Overhead State Retention Flip Flop Utilizing Crystalline In-Ga-Zn Oxide Technology

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***Abstract*—CAAC-IGZO technology has been used to design SR FFs with zero area overhead which can retain their state without any static leakage. These use of this SR FF conjunction with power gating to realize ultra-low power consumption in large circuits has been demonstrated.**

I. Introduction

In modern digital circuits, the static power continues to take an increasingly larger part of the total power consumption [1]. To decrease the static power, it is possible to use *state retention flip flops* (SR FFs), which in turn can use high V_{th} Si-transistors with a low off-state current to realize state retention with low leakage during power gating. These SR FFs can be used in conjunction with power gating to achieve low power consumption of large circuits.

Most SR FFs require a large area overhead, needs both switched power and always-on power and still experiences current leakage during power-gating applications [1]. While a solution consisting of SR FFs utilizing magnetic tunnel junction technology solves some of these problems, it brings additional complexity to system design, such as the use of plural control signals [2].

We propose a new SR FF utilizing *c-axis aligned crystal In-Ga-Zn Oxide* (CAAC-IGZO) technology. With an extremely low off current on the order of 10^{-24} A [3] [4], IGZO *thin-film transistors* (TFTs) can be used to enable state retention in a standard master-slave flip flop without adding extra area nor increased complexity to the control scheme.

II. Proposed State Retention Flip Flop

Fig. 1 shows the circuit schematic of our IGZO SR FF which has been fabricated and simulated. It consists of a master-slave flip flop, with the addition of an IGZO TFT and a retention capacitor (CAP) in the master latch. The IGZO TFT and the retention capacitor are stacked upon the Si-device layer and thus, there is no increase in area compared against a reference design. Fig. 2 shows another IGZO SR FF architecture which has been simulated for comparison purposes. The retention circuit is in parallel and includes both Si FETs and an IGZO TFT, allowing higher performance but an increased area overhead and more complex power control.

Table I shows some simulated performance metrics for the proposed series SR FF in Fig. 1 and the parallel type in Fig. 2 versus a reference FF without a state retention circuit. All metrics are for a Si W/L of 0.8 µm/0.35 µm and an IGZO W/L of 8 µm/0.8 µm for the series SR FF and an IGZO W/L of 0.8 µm/0.8 µm for the parallel SR FF. V_{DD} is 2.5 V and the retention capacitance is 0.1 pF. E_{avg} is calculated for a switched input value every clock cycle.

III. Implementation in Normally-Off CPU

To demonstrate the applicability of our series IGZO SR FF, we have implemented it in a 32-bit Normally-Off CPU where it achieved simple power gating at the target frequency of 15 MHz, making the IGZO SR FF suitable for ultra-low power microcontrollers.

References

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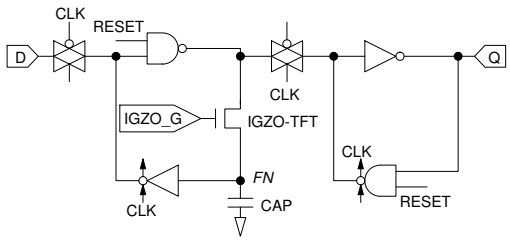

Fig. 1. A series IGZO SR FF architecture without area overhead.

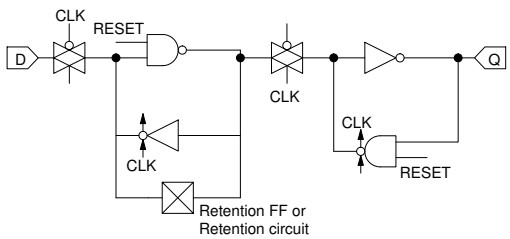

Fig. 2. A parallel IGZO SR FF architecture with area overhead.

TABLE I
Comparison between different FFs.

Type	f_{max}	E_{avg}	t_{backup}	E_{backup}	$t_{recovery}$	$E_{recovery}$	*Controllability*	*Area Overhead*
Reference FF	1.32 GHz	1.64 pJ	N/A	N/A	N/A	N/A	N/A	N/A
Series SR FF	0.05 GHz	1.81 pJ	0 s	0 J	0.548 ns	0.735 pJ	◯	0 %
Parallel SR FF	1.28 GHz	1.73 pJ	0.26 µs	0.89 pJ	1.08 ns	2.26 pJ	△	13.5 %