

Investigation of Si(110) surface roughness on MOS capacitor with ultrathin HfON gate insulator formed by ECR plasma sputtering

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1. Introduction

We have reported the effect of Si surface roughness on 3-D MOS capacitor with ultrathin HfON gate insulator formed by ECR plasma sputtering [1]. By annealing in Ar/4.9%H₂ ambient, the 3-D surface roughness was remarkably decreased and the electrical characteristics of 3-D MOS capacitor were improved. In 3-D MOS capacitor, the sidewall was different crystalline orientation such as (110).

In order to investigate the leakage current on 3-D MOS capacitor, we investigated the effect of Si(110) surface roughness on MOS capacitor with ultrathin HfON gate insulator formed by ECR plasma sputtering.

2. Experimental procedure

P-type Si(110) wafers were cleaned by SPM and DHF. After cleaning, the wafers were annealed in Ar/4.9%H₂ ambient to reduce the Si surface roughness at 700-1000°C (1 h) [2]. After flattening process, 2 nm-thick HfN film was deposited by ECR plasma sputtering at 0.19 Pa (Ar/N₂ : 20/1 sccm, μ -wave/RF power : 500/500 W). In order to form HfON, ECR Ar/O₂ plasma oxidation (0.10 Pa, Ar/O₂ : 10/4 sccm, μ -wave power : 300 W) was carried out for 3 s. After the plasma oxidation, 600°C post deposition annealing (PDA) was carried out for 1 min in N₂ ambient. The fabricated HfON film thickness was about 4 nm. Finally, backside Al electrodes were formed by thermal evaporation.

3. Results and Discussion

The surface roughness of p-Si(110) substrate was remarkably reduced by annealing in Ar/4.9%H₂ ambient especially at 1000°C. The RMS roughness for the p-Si(110) surface of without (w/o) annealed (0.22 nm) was decreased to 0.087 nm for Ar/4.9%H₂ annealing. In case of p-Si(100), the RMS roughness for the surface of w/o annealed Si (0.20 nm) was decreased to

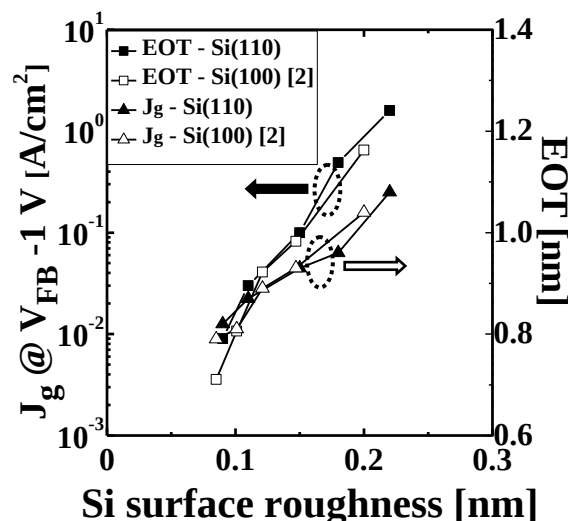


Fig. 1 The p-Si(110) and p-Si(100) surface roughness dependence on EOT and J_g.

0.085 nm for Ar/4.9%H₂ annealing. It was found that the flat p-Si(110) surface makes the EOT (@ 100 kHz) smaller from 1.1 nm (w/o annealed Si) to 0.82 nm (Ar/4.9%H₂ annealed Si at 1000°C), while it was decreased from 1.0 nm to 0.79 nm in case of p-Si(100). By reducing the Si surface roughness, the leakage current densities were decreased from 1.2×10^0 A/cm² to 7.8×10^{-3} A/cm² for the p-Si(110) and from 6.5×10^1 A/cm² to 3.5×10^{-3} A/cm² for the p-Si(100).

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References

- [1] D. H. Han and S. Ohmi, The 60th JSAP spring meeting, 28p-G8-6, p. 13-018, 2013.
- [2] D. H. Han and S. Ohmi, IEICE TRANS., Vol. E96-C, No. 5, pp. 669-673, 2013.