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Characterization of Interface Traps in Au/Al_2O_3/GeO_x/Ge MOS Structures

Ju-Chin Lin[1], Rui Zhang[1, 2], Noriyuki Taoka[3], Mitsuru Takenaka[1] and Shinichi Takagi[1]

[1]School of Engineering, The University of Tokyo, 2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-8656, Japan

[2]School of Electronic Science and Engineering, Nanjing University, 22 Hankou Road, Nanjing 210093, China

[3]Graduate School of Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan

Tel: +81-3-5841-6733, Fax: +81-3-5841-8564, E-mail: shizuka@mosfet.t.u-tokyo.ac.jp

Introduction A plasma post oxidation method has been proposed to form an ultrathin GeO_x IL through a thin ALD Al_2O_3 layer using ECR oxygen plasma exposure and has been demonstrated to realize low D_{it} and high MOSFET mobility with maintaining ultrathin GeO_x [1, 2]. However, further reduction of the Ge MOS interface traps is still a crucial issue. It is quite important to establish the physical understanding of the electrical properties and the origin of the GeO_x/Ge interface traps.

In this study, the conductance method performed in a wide measurement temperature range reveals that three types of traps exist in Al_2O_3/GeO_x/n-Ge MOS interfaces, fabricated by plasma post oxidation.

Experiment N-type Ge substrates with (100) orientation were pre-cleaned before deposition of 1-nm-thick Al_2O_3 by ALD at 300 °C. Subsequently, the plasma post oxidation was carried out for these Al_2O_3/Ge structures at substrate temperature of 300 °C. The second ALD of 2-nm-thick Al_2O_3 was performed on the Al_2O_3/GeO_xGe samples. After PDA in N_2 ambient for 30 min at 450 °C, Au gate electrodes and Al back contacts were formed by thermal evaporation.

Results and discussion Conductance measurements were performed on the MOS capacitor at 162, 172, 213, 235, 253, 272 and 291 K. Fig. 1 and Fig. 2 show the measured conductance curves of the sample at 172 and 253 K, respectively. It is observed in Fig. 1 (a) that, as the surface potential moves toward the conduction band edge (E_c), the peak (solid curves) shifts towards higher frequency. On the other hand, the conductance peak in Fig.1 (b) (dashed curves) shifts towards lower frequency, indicating that this trap (Trap B) has a different physical origin from the one in Fig. 3 (a) (Trap A). In Fig. 2 (a), a new set of the peaks (dotted curves), whose frequency has much smaller variation with changing the surface potential, are observed. In Fig. 2 (b) the peaks similar to the ones in Fig. 1 (b) are observed again.

In Fig. 3 (a), the increase in the peak frequency of Trap A with increasing the surface potential indicates that this trap can be regarded as a normal fast interface trap communicating with free electrons. In contrast, the surface potential dependence of the peak frequency in Trap B is fully opposite even in the surface potential close to E_c. The possible physical origin of this trap is a boarder trap whose density has a specific depth profile. In Fig. 3(b) the peak frequency in Trap C gradually increases with an increase in the surface potential, suggesting the communication with electrons.

In Fig. 4 (left) the cross section of Trap A is almost independent of the surface potential and temperature, which is the common feature observed in fast trap in Si MOS interfaces. The cross section of Trap C is much smaller than that of Trap A. This finding suggests that the physical origin of Trap C can be a slow trap inside the gate insulators, where majority carrier electrons are trapped through tunneling into the GeO_x IL. Also, the cross section of trap C is found to decrease with an increase in the surface potential, which might be related to the depth of the border traps from the MOS interface.

Fig. 4 (right) shows the energy distributions of trap density (D_{it}) of Trap A, B and C, determined by fitting the calculated conductance curves to the measured ones. D_{it} of Trap A is in lower half of 10^{11} cm^{-2} eV^{-1} order, which is consistent with the previous results [1].

Conclusion Three types of traps have been detected in Al_2O_3/GeO_x/n-Ge MOS interfaces by using the conductance method at temperatures from 162 to 291 K. The properties of these traps have been characterized through analyses of the peak frequency, the capture cross section, and the D_{it} distributions.

References [1] R. Zhang, et al., *Appl. Phys. Lett.*, 98, 112902 (2011) [2] R. Zhang, et al., *IEEE Trans. Electron Devices*, 59, 335 (2012)

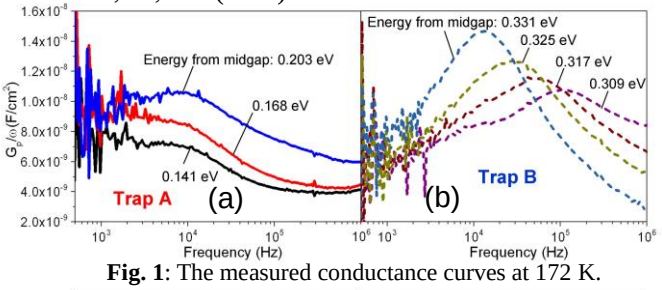

Fig. 1: The measured conductance curves at 172 K.

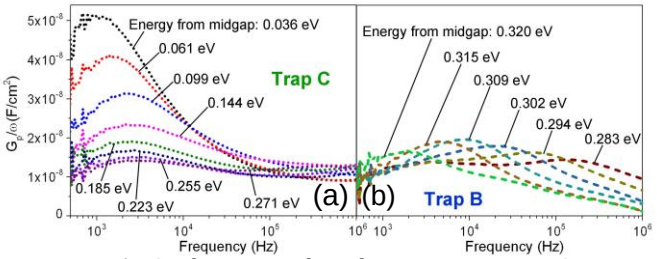

Fig. 2: The measured conductance curves at 253 K.

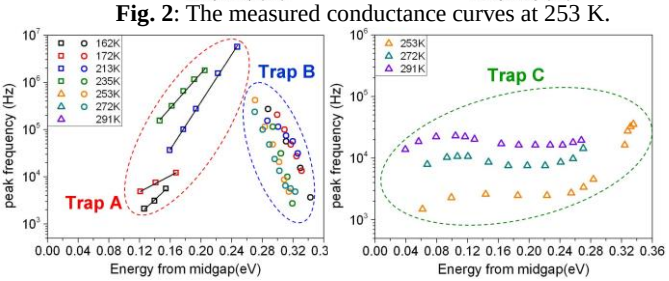

Fig. 3: The energy distributions of the peak frequency of (a) Trap A and B, shown in Fig. 3, and (b) Trap C, shown in Fig.4.

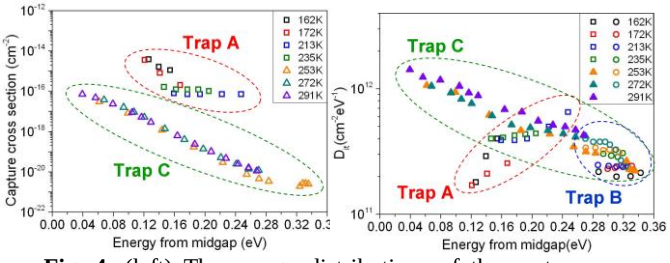

Fig. 4: (left) The energy distributions of the capture cross sections extracted from the peak frequency.
(right) D_{it} distributions of the Au/Al_2O_3/GeO_x/Ge MOS capacitor.