Performance Degradation Due to Drain-Induced Barrier Lowering in Ultra-Low Supply Voltage CMOS Circuits Operating in Subthreshold Region

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[Introduction] Drain-induced barrier lowering (DIBL) which affects circuit performance and SRAM is one of the short channel effects and has increased recently, especially in scaled bulk MOSFETs [1-4]. As DIBL increases, effective current (I_{th}) decreases and circuit delay is largely degraded even if on-current (I_{on}) is the same [1, 2]. In the subthreshold region, devices are more sensitive to the V_{th} change than in normal V_{dd} operation, and therefore, the effect of DIBL may be more severe in the subthreshold circuits. In this work, the impact of DIBL on subthreshold devices and circuits is examined. Two transistors with a small and large DIBL are measured and ring oscillators are simulated assuming different values of DIBL. Results show that the effects of DIBL are more significant in subthreshold region than in the above-threshold region.

[Results and Discussion] Two transistors in 1k nFETs by the 65 nm technology with almost the same I_{on} and I_{off} but very different DIBL are selected in order to analyze the DIBL effect on actual device. Fig. 1 shows measured I_{ds}/I_{on} as a function of V_{ds}/V_{dd} at V_{dd} ranging from 0.1 V to 1.2 V in case of large DIBL. The I_{ds}/I_{on} changes drastically with V_{dd} and it is also shown in the fig. 2 compared with small DIBL. It is found that, in the large DIBL transistor, I_{ds}/I_{on} reaches the minimum point at 0.3 V and 0.4 V. These results indicate that DIBL heavily affects the subthreshold characteristics compared with the above-threshold region. In order to investigate the effect of DIBL on circuit performance, CMOS ring oscillators which is composed of the five sets of transistors (A-E) with different DIBL are simulated in various V_{dd}. Fig. 3 shows simulated output characteristics of transistors with various DIBL in subthreshold region (V_{dd} = 0.3 V). I_{ds}/I_{on} at V_{ds}/V_{dd} = 0.5 decreases with increasing DIBL and note that DIBL dependence is very similar to measured data in Fig. 1. Fig. 4 shows normalized delay time of CMOS ring oscillator. Although the delay degradation in “E” is less than 30% at 0.6V, it reaches approximately 80% at 0.3V, which is the subthreshold region. It is clearly shows that the impact of DIBL is severe on subthreshold CMOS circuits.

[Conclusion] A transistor with a large DIBL has apparently I_{th} and delay degradation in the subthreshold region. Therefore, it is highly required to suppress DIBL in the design of high energy efficiency CMOS circuits in the subthreshold region.

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