19a-P5-12

Electrical Characteristics of Ge/Si Hetero-Junction Tunnel Field-Effect Transistors and their Post Annealing Effects

Minsoo Kim, Yuki Wakabayashi, Ryosho Nakane, Masafumi Yokoyama,
Mitsuru Takenaka and Shinichi Takagi
The Univ. of Tokyo
E-mail: minsoo@mosfet.t.u-tokyo.ac.jp

1. Introduction

Tunnel field-effect transistors (TFETs) have attracted much attention as a strong candidate for future generation transistors because of the scalability of supply voltage [1]. However, there are many challenges to satisfy the theoretical expectations. One of the feasible solutions for mitigating the present problem is to employ a Ge/Si hetero-junction structure [2]. In this paper, we report the fabrication of Ge/Si hetero-junction TFETs and post annealing effects on the electrical characteristics.

2. Experiment

A 10-nm-thick silicon-on-Insulator (SOI) substrate was used for a starting material. Phosphorus ion implantation at low energy of 3 keV was carried out to form the drain, followed by RTA at 900 ^{o}C for activation. A 33-nm-thick Ge layer was grown at 200 ^{o}C on the drain regions formed in the SOI substrate with in-situ boron-doping by molecular beam epitaxy. The doping concentration in the Ge layer was estimated from the resistivity to be as high as 1.3×10^{20} cm^{-3}. 2-step 4-nm-thick Al_2O_3 was formed by atomic layer deposition with electron cyclotron resonance (ECR) plasma post oxidation to ensure the high quality MOS interface between Al_2O_3 and Ge [3]. Ta was deposited as the gate metal, followed by Ni and Al deposition for the source contact and the contact pad, respectively. Furnace annealing in nitrogen ambient from 200 ^{o}C to 400 ^{o}C for 30 min were carried out to examine post annealing (PA) effects on the electrical characteristics.

3. Results and Discussion

After PA, higher on/off current ratio (I_{on}/I_{off}) and steeper SS were obtained in small drain voltage (V_d=0.1 V). As the PA temperature increases, the off-current decreases with maintaining constant I_{on}, leading to the increase in the I_{on}/I_{off} ratio. It is found that SS is also enhanced by increasing the PA temperature and steep SS_{min} below 60 mV/dec is obtained at 400 ^{o}C PA. In order to study the origin of the performance enhancement by PA, the electrical characteristics of control Si-MOSFETs fabricated on the same wafer with identical processes as the Ge/Si hetero-junction TFETs, were evaluated. The I_d-V_g characteristics and SS of Si-MOSFETs are improved with increasing the PA temperature, as similar to those of TFETs. The interface state density (D_{it}) between Si and Al_2O_3-gate insulator extracted from SS is reduced by PA. These results mean that the decrease in the off-current and SS in control Si MOSFETs is attributable to the improvement of D_{it}.

3. Conclusions

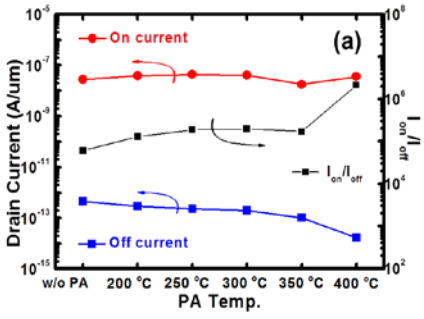
A Ge/Si hetero-junction TFET with in-situ boron doped Ge epitaxy was demonstrated. A high performance of steep SS below 60 mV/dec and large I_{on}/I_{off} ratio over 10^6 was realized by the proper PA process. It was found that D_{it} between Al_2O_3 and Si in the channel region is a critical factor for high performance Ge/Si hetero-junction TFETs.

Acknowledgements

This work was technical supported by Prof. Tanaka, and Prof. Ohya for in-situ boron doped high quality Ge growth.

References

[1] A. M. Ionescu and H. Riel, Nature 479 (2011) 329. [2] F. Mayer, Tech. Digest IEEE Int. Electron Devices Meet. (2008) 1. [3] R. Zhang et al., IEEE Trans. on Electron Devices 59 (2012) 335.



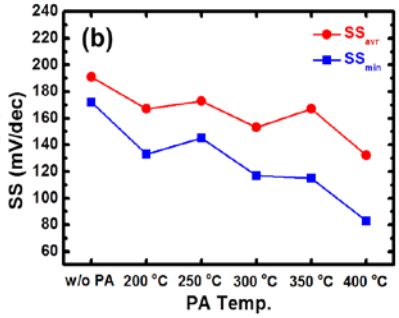


Fig.1 (a) I_{on}/I_{off} ratio and (b) subthreshold swing of the Ge/Si hetero-junction TFET versus PA temperatures.

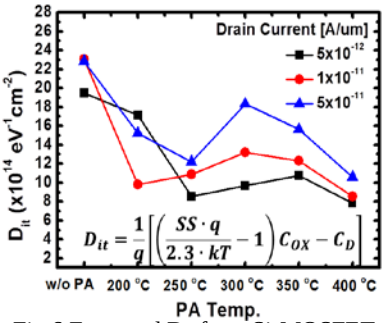


Fig.6 Extracted D_{it} from Si-MOSFETs