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Photocarrier Buildup Effects in Si Nanostripes Measured by Scanning Probe Microscopy

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In modern systems, compact photosensors operating at low voltage are highly desirable for integration with on-chip optical interconnect networks. Previously, we have demonstrated twofold photocurrent increase at edges of Si stripes due to light absorption at top and side surfaces measured by multimode scanning probe microscopy (SPM).[1] Here, we examined photocurrent increase due to charge buildup at edges of rectangular Si stripes (Si(001), ~1E17 cm^{-3}) under optical excitation with 364 nm laser light.

To observe effects of the charge buildup, Si stripes were exposed to modulated laser light at ~40° angle, resulting in illumination of top and left side of the stripes. While SPM topographs were acquired in a constant-force mode, photocurrent amplitude (PC), i.e. the probe-sample current, was measured by a lock-in technique at a sample voltage of V_S =-0.8 V. The Si surfaces were passivated by ultrathin oxide.[2]

For light with λ=364 nm, the PC peak/interior ratio was ~4.5 for a line profile in Fig.1(b). For different stripes, the PC ratio between 1 and 10 was measured.[Fig.1(d)] Simulation results of the photocarrier distribution in a Si bar including carrier collection depth and diffusion gave a PC ratio of ~2 for incoherent light,[Fig.1(c)] and ~4 when light interference was included. For the junction under illumination, the band-bending potential(V_{bb}) and the collection depth decreased due to surface charge buildup, which resulted in increase of the gap potential(V_{gap}) and, consequently, the SPM current as illustrated in Fig.1(a). Simulations of V_{gap} (not shown) suggested that the PC grew super linear with V_{gap} and, thus, contribute to further increase in the PC ratio. Because the carrier buildup depends on geometry of the Si stripe, and the detail balance of photocarrier generation and recombination processes, the PC ratio was used as a measure of the stripe quality. The results showed effective photocarrier buildup for defect-free, sharp Si stripe edges.

[1] L.Bolotov, et al., JJAP **51**, 088005 (2012); [2] L.Bolotov et al., JVSJ **54**, 412 (2011)

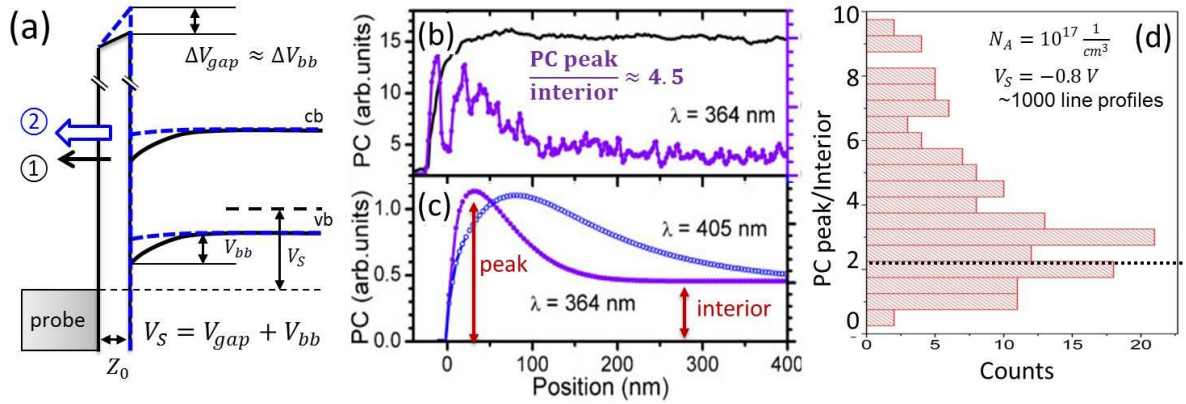

Fig.1 (a) Energy band diagram of SPM junction and SPM current: in dark (black, ①) and under illumination (blue, ②). (b) Measured line profiles crossing the Si stripe edge: height (black line) and PC (violet line). (c) Calculated PC profiles from ref.[1] (d) The PC ratio at V_S=-0.8V for different Si stripes.