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Bumpless 3D Interconnects for the Tera-scale Bandwidth and High Density Devices Equivalent to <10nm Node Scaling

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The key features are bumpless interconnects in the three-dimensional integration (3DI) for Chip-on-Wafer (COW) and Wafer-on-Wafer (WOW) as a second-generation alternative to the use of micro-bump based Chip-on-Chip (COC) as shown in **Figure 1**. Wafer-based 3D technologies are the fabrication of three-dimensional structures in which any number of thinned 300 mm wafers can be stacked back-to-front realizing further large-scale devices with low cost instead of the scaling using extreme ultraviolet (EUV) lithography and bump based COC 3D integration.

The two-dimensional (2D) scaling based on planar technology that has led the semiconductor industry so far no longer makes economic sense in many situations. For instance, the industry is facing a major turning point in how to realize the next generation of large-scale integration. In this context, 3D approaches have been proposed on the basis of next-generation 2D transistors and 3D architectures, and recent attention has focused on productivity and the costs involved in volume production. Transistor-based 3D (stack structure by transistors) will face to yield drawbacks due to increasing invisible defect at the critical layers.

Stacking at the wafer level drastically increases the processing throughput, and bumpless interconnects as well as Through-Silicon-Via (TSV) provide >10K/cm^2 IO counts and an appropriate yield using existing technology which is equivalent to or greater than that achievable with 2D scaling beyond 22 nm nodes. Also, since it is compatible with existing wafer processing facilities, transistors with three-dimensional structures can be designed in a continuous manufacturing line.

WOW is classified into two types, according to the stacking method: *Thinning first* and *Via-Last after Bonding*. The development has proceeded through four modules, classified along the process flow. The modules include a *thinning module* for thinning down to 10 μm the wafer substrates in which devices are implemented, a *stacking module* for bonding and stacking the wafers, a *interconnects module* for forming Cu interconnects embedded in upper and lower wafers with via-holes, and a *packaging module* for singulating the stacked wafers. Damascene interconnects form a so-called redistribution layer and also serve as a counter electrode for the subsequent stacked wafer.

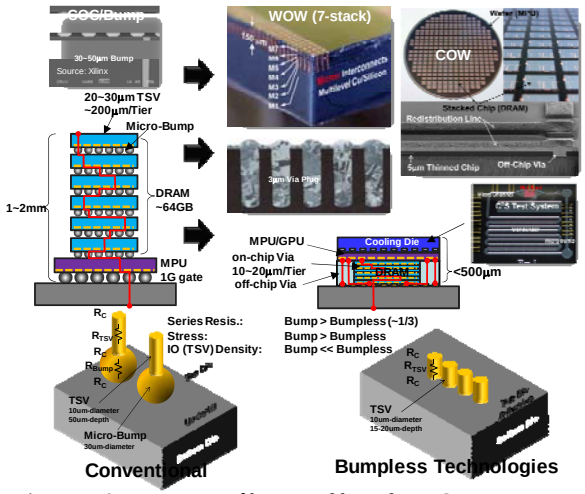

Figure 1. A comparison of bump and bumpless TSV interconnects for 3D logic/memory stack structures, assuming six dies for a memory stack and one many core microprocessor. Bumpless TSVs can form with high dense (narrow pitch) rather than TSV+ bump which provides large enough IO counts. Since back-to-front stack and TSV-last process has no limit on the multi-stacking, high density and bandwidth more than Tera-scale can be anticipated using matured existing devices.

In combination with 3D logic and memory, it is possible to construct a roadmap towards high-density integration and miniaturization of 3D chip-sets, especially next-generation logic-memory stacks for personal digital assistants (PDAs) and Smartphones. Because wafer thinning to 10 μm or less provides small features, it is possible to realize a total 3D stack height of 1000 μm, even after stacking 100 dies. This satisfies current package standards. Stacking 32 or more layers of 16 Gb/cm^2 devices fabricated by 22 nm technology would achieve terabit (Tb) capacity, which is equivalent to <10 nm three generations ahead as shown in **Figure 2**. Thus the manufacturers can choose one among scaling, wafer enlargement, and 3D stack, taking total cost into account.

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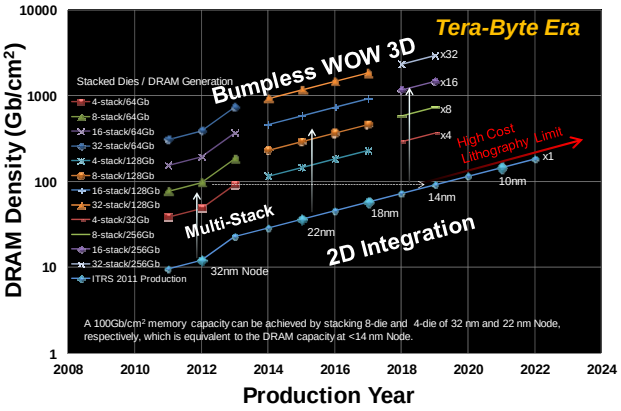

Figure 2. Trends toward DRAM density using 2D conventional scaling and 3D multi stack using existing DRAM generation. DRAM capacity in the 3D corresponds to the number of stacked dies, assuming to eliminate redundancy by cell-block at each layer.