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Room Temperature Memory Operation in a Solid-State Device based on Thiol-Functionalized Oligo(Phenylene-Ethynylene)-Protected Gold Nanoparticles

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We have established a fabrication process for nano-scaled solid-state devices using the combination of top-down and bottom-up methods. Our capability in the production of gold (Au) few nanometer gap-sized nanogap electrodes and the chemisorption of alkanethiol protected Au nanoparticles (Au NPs), porphyrin derivatives between the electrodes, resulted in the demonstration of single electron transistors (SETs) and memory operation in solid-state molecular devices at room temperature (RT) [1,2]. In this work, we synthesized and introduced thiol-functionalized oligo(phenylene-ethynylene) (OPE) protected Au NPs between the nanogap electrodes [3] and demonstrate the reproducible memory operation at RT.

Au nanogap electrodes with 3.6 nm in gap separation were fabricated by using electron beam lithography (EBL) and molecular ruler electroless gold plating (MoREP) [4]. The nanogap electrodes were immersed into the thiol-functionalized OPE protected Au NP (core average diameter size of 2.1 nm) solution. The electrical measurements were carried out at RT.

Figure 1 shows the current-voltage (*I-V*) characteristics applying forward and backward bias voltage sweeps to the device. Negative differential conductance (NDC) is observed when the conductance changes from the high to the low states. The current response shows a clear hysteresis implying two different states at -0.5V. For the observation of switching behavior, writing, reading and erasing voltages were set at +0.6 V, -0.4 V and -1.0 V respectively. In figure 2, reproducible memory operation of the solid-state device is demonstrated at RT.

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[1]. Daniel Hurtado, Y. Majima et al., *The 73th Autumn Meeting of JSAP*, 12p-C8-4 (2012).
[2]. Daniel Hurtado, Y. Majima et al., *The 73th Autumn Meeting of JSAP*, 11p-H1-13 (2012).
[3]. Hyunmo Koo, Y. Majima et al., *Appl. Phys. Lett.* **101**, 083115 (2012).
[4]. S. Takeshita, Y. Majima et al., *The 59th Spring Meeting of JSAP*, 17p-GP8-12 (2012).

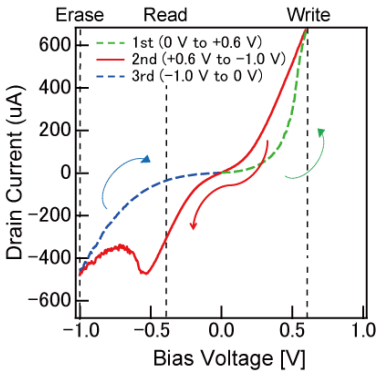

Fig. 1 *I-V* characteristics of thiol-functionalized OPE Au NP device.

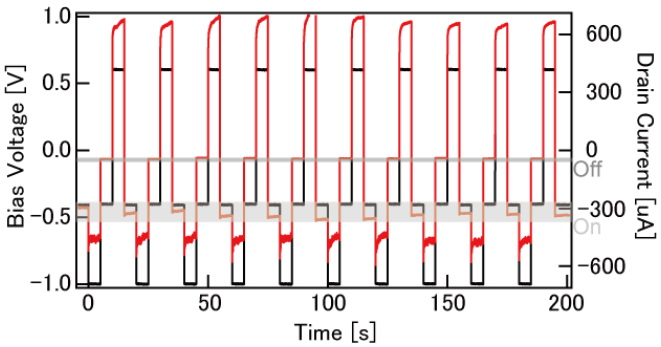

Fig. 2 Pulse sequence of the memory operation. Black solid line: voltage, red solid line: current.