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Improvement of Al_2O_3/InGaAs Interfaces by Ultrathin Ga Oxide Passivation

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Recently, high-k/III-V interface control has been investigated extensively for MOSFET applications. Previous studies have shown that the interface GaO_x species on GaAs and InGaAs surfaces may be the most important key issue for III-V interfacial control [1-5]. Analogy to Al_2O_3 ALD using the $Al(CH_3)_3$ (TMA) precursor would suggest GaO_x growth by using $Ga(CH_3)_3$ (TMG). However, ALD of GaO_x films using TMG is known to be difficult [6]. In this paper, we report the growth of ultrathin GaO_x layer using TMG and the impact of GaO_x passivation on $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structure.

GaO_x growth carried out by repeating the cycle of TMG and H_2O supplies at 250 °C. The oxide thicknesses were measured by spectroscopic ellipsometry with using the reference refractive-index data for Ga_2O_3. GaO_x growth on GaAs and InGaAs substrates could be detected when the deposition was continued for more than 30 cycles. The GaO_x film thickness was becoming saturated at ~0.40 nm with the deposition cycle of up to 150 cycles. These results revealed that ultrathin GaO_x layers can be grown while thick GaO_x films could not be formed. With 30-cycle GaO_x ALD growth, XPS spectra confirmed the monolayer growth on InGaAs surface. GaO_x thickness from XPS measurement was 0.11 nm, which was consistent well with ellipsometry result. Using TMG, self-limiting growth of ultrathin GaO_x layer on GaAs and InGaAs substrates can be realized. Self-cleaning effect of AsO_x by TMG was also observed similarly to TMA.

We investigate the effect of ultrathin interfacial GaO_x layer on the Al_2O_3/InGaAs MOS structure. Prior to ALD, the n-InGaAs/InP(100) substrates were treated in NH_4OH solution for 1 min and rinsed in deionized water. GaO_x and Al_2O_3 deposition was carried out consecutively at 250 °C. The deposition cycle number of GaO_x was varied from 0, 30 and 50. Post deposition annealing was done in vacuum at 400 °C for 2 min and the post metallization annealing was performed in Ar at 350 °C for 2 min. Figure 1 shows C-V characteristics for (a) ALD-Al_2O_3 (10 nm)/InGaAs, (b) ALD-Al_2O_3 (10 nm)/30-cycle ALD-GaO_x/InGaAs, and (c) ALD-Al_2O_3 (10 nm)/50-cycle ALD-GaO_x/InGaAs structures with Au electrodes. 30-cycle GaO_x interface layer reduced capacitance under the negative bias, but 50-cycle one bounded back these capacitances. Frequency dispersions around V_{fb} and under accumulation were slightly affected by the GaO_x insertion as compared to the control sample. Figure 2 shows interface trap density (D_{it}) with different GaO_x deposition cycles, estimated by conductance method [assuming $D_{it} = 2.5/q \times Gp/\omega$]. It is clear that D_{it} around the midgap of InGaAs bandgap was reduced extensively by 30-cycle GaO_x insertion. Minimum D_{it} as low as 2.4×10^{11} $cm^{-2}eV^{-1}$ was achieved. MOSFET performances also showed the improvement of effective mobility by ultrathin GaO_x passivation. This study is granted by JSPS through FIRST program initiated by CSTP.

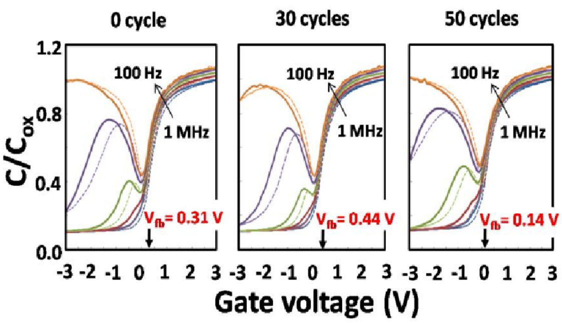

Fig. 1 C-V characteristics of (a) ALD-Al_2O_3 (10 nm)/ InGaAs, (b) ALD-Al_2O_3 (10 nm)/30-cycle ALD-GaO_x/InGaAs, and (c) ALD-Al_2O_3 (10 nm)/50-cycle ALD-GaO_x/InGaAs structures with Au electrode.

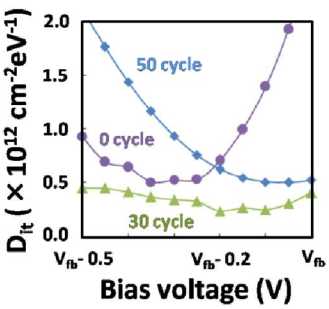

Fig. 2 Comparison of interface trap densities (D_{it}) with different GaO_x passivation cycle of 0, 30, and 50 cycles.

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