

Formation of sub-10nm nanoholes by two-step anodization of aluminum on silicon substrate

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Abstract

Arrays of silicon nanowires are promising for electronic[1] and opto-electronic[2] applications thanks to large surface to volume ratio as well as quantum size effect. Among various methods to fabricate silicon nanowires, vapor-liquid-solid (VLS) growth is one of the most popular techniques that require the use of a metallic catalyst. Gold is the most selected one due to low Si-Au eutectic temperature. However, the distribution of gold catalyst is almost randomly dispersed on silicon substrate. Using the anodic aluminum oxide (AAO) via electrochemical gold deposition on silicon substrate is referred to improve the homogeneous distribution of gold catalyst. The pore diameters of AAO control the size of gold catalysts as well as the diameter of the subsequently grown silicon nanowires. In this contribution, we will focus on self-ordered AAO template fabrication on silicon substrate using well-known two step anodizing process in sulphuric acid electrolyte. By monitoring the anodization current during the electrochemical process as a function of time, the pore diameters of AAO were controlled. Small pore diameters in range of about 8-20nm were obtained by applying a low anodizing potential 5-12V [Figure 1a]. Further working is aimed to deposit gold molecules inside the sub-10nm cylinder structure of AAO template by electrochemical plating method. Gold nanowires with sub-10nm diameter are formed by firstly proceeding long plating duration and subsequently using chemical wet etching with AAO template [Figure 1b].

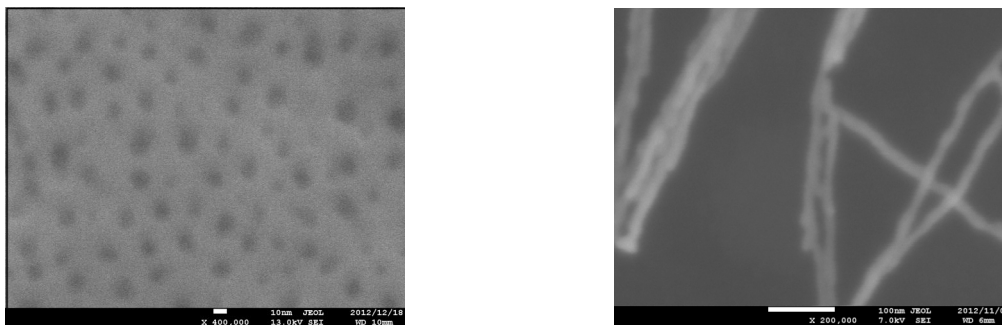


Figure 1: SEM images depicting: **a)** AAO template fabricated at anodized voltage 6V; **b)** gold nanowires formed at plating voltage 3V.

References

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