28p-G11-6

# Field Isolation of GaN MOSFET by Boron Ion Implantation

The Univ. of Tokushima[1], Dalian Univ. of Tech.[2], Kyushu Inst. of Tech.[3], SAMCO Inc.[4]
°Ying Jiang[1,2], Qingpeng Wang[1,2], Kentaro Tamai[1], Satoko Shinkai[3], Takahiro Miyashita[4],
Shin-Ichi Motoyama[4], Dejun Wang[2], Jin-Ping Ao[1], and Yasuo Ohno[1]
E-mail: yjiang@ee.tokushima-u.ac.jp

GaN MOSFETs are being developed to achieve enhancement-mode (E-mode) operation [1]. However, the device isolation is still not developed. The region is called “field region” and should be non-conductive even in case of high voltage wiring running over the region. In this paper, we report the investigation on the device isolation processes for GaN MOSFETs by three technologies, boron ion implantation (B I/I), Ni diffusion and reverse sputtering treatment.

GaN MOSFETs were fabricated on AlGaN/GaN heterostructure where gate region is formed by the removal of the AlGaN layer (Fig. 1). Ring-type MOSFETs with inner and outer gate electrode radii of 89 μm and 183 μm ($L$=94 μm, $W_{eff}$=819 μm) were used for the conductivity evaluation. There are two patterns on the chips, normal gate MOSFET and field MOSFET. In the fabrication process, field isolation was first done with different isolation conditions, which were ICP dry etching with the gases of $SiCl_4/Cl_2$ or $BCl_3/Cl_2$, with or without B I/I, Ni diffusion and reverse Ar sputtering in sputtering chamber. After the etching, B ions were double implanted to some samples with the energy, dose of 30 keV, $5\times10^{14}$ $cm^{-2}$ and 110 keV, $7\times10^{14}$ $cm^{-2}$, respectively. The mask for I/I was the double layers of 500 nm $SiO_2$ and 2 μm photoresist. For another samples, 100 nm thick Ni was sputtered, lifted-off and annealed at 850 °C for 30 min in $N_2$ ambient as drive-in diffusion. Then, Ni was removed by aqua regia. The reverse sputtering treatment with Ar plasma was done for 30 min with the power of 180 W. Then, the gate region was etched by ICP with $SiCl_4$ at a lower etching rate to reduce the etching damage. After gate region etching, silane-based $SiO_2$ (100 nm) was deposited as gate oxide for both normal gate and field FETs, and annealed at 1000 °C for 10 min in $N_2$ ambient. The ohmic contacts were formed using Ti/Al/Ti/Au (50/200/40/40 nm) annealed at 850 ºC for 1 min in $N_2$ ambient. The gate metal was formed using Ni/Au (70/30 nm) both for normal gate and filed FETs again.

The devices of normal gate FETs demonstrated an electron mobility of about 140 $cm^2V^{-1}s^{-1}$ [1]. The field FETs without any special treatments showed E-mode operation (Fig. 2) with electron mobility of about 120 and 135 $cm^2V^{-1}s^{-1}$ for the devices etched with $SiCl_4$ and $BCl_3$, respectively. The devices with Ni diffusion and reverse sputtering had large oxide leakage and cannot be measured the transistor characteristics. The devices with boron ion implantation showed low drain currents and no change with the gate bias. In addition, no deterioration of electron mobility and no threshold voltage variation were observed from the normal gate FETs on the same chips.

In conclusion, B I/I is an effective method to obtain good device isolation for GaN MOSFETs.

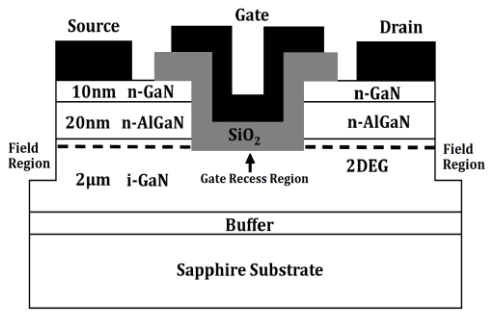


Fig. 1 Device structure of GaN MOSFETs

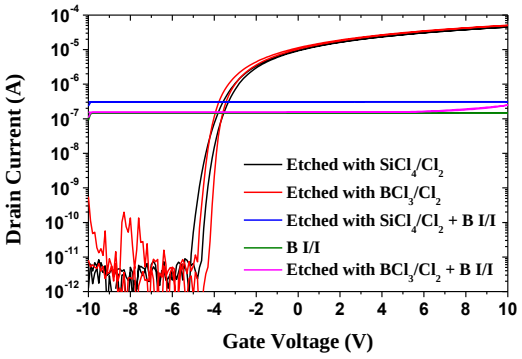


Fig. 2 Transfer characteristics of ring-type MOSFETs formed in field region.

## References

[1] Q. Wang: Jpn. J. Appl. Phys **52**, (2013) (in press).