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High Mobility Ge CMOS devices with 0.7 nm Ultrathin EOT using $HfO_2/Al_2O_3/GeO_x$/Ge Gate Stacks Fabricated by Plasma Post Oxidation

Rui Zhang, J. C. Lin, P. C. Huang, N. Taoka, M. Takenaka and S. Takagi
School of Engineering, The University of Tokyo, 2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-8656, Japan.
Tel: +81-3-5841-6733. E-mail: zhang@mosfet.t.u-tokyo.ac.jp

Introduction Ge MOSFETs have been attracting a lot of interest for further improvement of the CMOS performance [1]. For high performance Ge MOSFETs, a gate stack with both low D_{it} and thin EOT is mandatory [2]. A plasma post oxidation (PPO) method has been purposed by using ECR oxygen plasma to fabricate Al_2O_3/GeO_x/Ge gate stacks with low D_{it} at 10^{11} $cm^{-2}eV^{-1}$ order and thin EOT of ~1 nm [3-5]. However, further EOT reduction of the Al_2O_3/GeO_x gate stacks is difficult, due to the relatively small permittivity of Al_2O_3 (7~9) and GeO_x (~5.5). In this research, $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks with EOT of ~0.7 nm are fabricated using the PPO method assisted by a 0.2-nm-thick Al_2O_3 layer between HfO_2 and Ge, with maintaining low D_{it}. The high mobility Ge (100) p- and n-MOSFETs using these gate stacks are also demonstrated.

Experiments The active areas were defined by etching SiO_2 field oxides formed on Ge (100) substrates. Subsequent to the sacrificial oxidation, the HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/GeO_x/Ge structures were prepared by 300 °C ALD and PPO for different times at RT. PDA was carried out at 400 °C for 30 min in N_2. TiN was deposited and ion implantation was done to form S/D for both p- and n-MOSFETs. After the activation annealing, Ni S/D contact metals were sputtered and the Al back contact was formed by thermal evaporation.

Results and discussion Fig. 1 shows a cross section TEM image of the $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks. It is found that a 0.35-nm-thick GeO_x interfacial layer (IL) was formed with a sharp GeO_x/Ge interface after PPO without inter-mixing with the HfO_2 layer, which has also been confirmed by AR-XPS measurements (data not shown). With this gate stack, low D_{it} of 2×10^{11} $cm^{-2}eV^{-1}$ is revealed under EOT of 0.76 nm.

The I_d-V_g characteristics shown in Fig. 2 are taken from the Ge p- and n-MOSFETs having an $HfO_2/Al_2O_3/GeO_x$/Ge gate stack with 15 s' PPO. Normal operations are confirmed for the p- and n-MOSFETs with an on/off ratio of ~10^4 and an S factor of 85 mV/dec for pMOSFET, and an on/off ratio of ~10^3 and an S factor of 80 mV/dec for nMOSFET. The mobility of the Ge p- and n-MOSFETs with different types of gate stacks, evaluated by the split C-V method, is shown in Fig. 3 and Fig. 4, respectively. It is found that with the PPO $HfO_2/Al_2O_3/GeO_x$/Ge gate stack, the Ge pMOSFET exhibits the hole mobility much higher than the Si universal one. The mobility with 0.76 nm EOT is comparable to or even higher than that of ~20-nm-thick thermal oxidation GeO_2/Ge gate stack [6]. For the Ge nMOSFET, the electron mobility is comparable to the Si universal one and exceeds it in high N_s region. The much higher mobility in the $HfO_2/Al_2O_3/GeO_x$/Ge gate stack than those in the direct HfO_2/Ge and the HfO_2/Al_2O_3/Ge interfaces indicates that the formation of the GeO_x/Ge interface is a key for realizing high mobility Ge p- and n-MOSFETs. The peak mobility of 546 and 689 cm^2/Vs are obtained for the Ge p- and n-MOSFETs with EOT of 0.76 nm, which are the highest reported peak mobility for Ge CMOS devices with sub-nm ultrathin EOT.

Conclusion The superior $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks were fabricated by applying the PPO method for HfO_2/Al_2O_3/Ge structures. These gate stacks exhibit ultrathin EOT of down to ~0.7 nm and D_{it} of 10^{11} $cm^{-2}eV^{-1}$ order. The Ge (100) p- and n-MOSFETs with these gate stacks have been demonstrated with superior electrical properties. As a result, the record high hole and electron mobility of 546 and 689 cm^2/Vs have been realized under EOT of 0.76 nm for Ge p- and n-MOSFETs, respectively.

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References [1] S. Takagi et al., IEDM, pp. 57, 2003. [2] S. Takagi et al., Microelectron. Eng., 84, pp. 2314, 2007. [3] R. Zhang et al, Appl. Phys. Lett., 98, 112902, 2011. [4] R. Zhang, et al. VLSI symp., pp. 56, 2011. [5] R. Zhang, et al., IEDM, pp. 642, 2011. [6] Y. Nakakita et al., IEDM, pp. 877, 2008. [7] K. Morii, et al. IEDM, pp. 681, 2009.

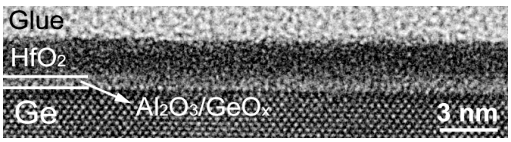

Fig. 1: TEM image of O_2 (2.2 nm)/Al_2O_3 (0.2 nm)/Ge structure with a 500 W PPO for 15 s.

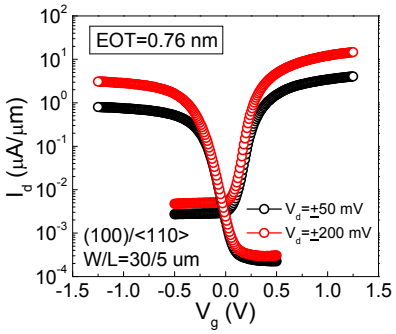

Fig. 2: I_d-V_g curve of the Ge p- and n-MOSFET with the $HfO_2/Al_2O_3/GeO_x$/Ge gate stack having 15 s' PPO.

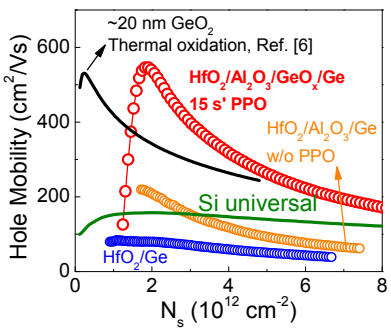

Fig. 3: Mobility of Ge pMOSFETs having different MOS interfaces.

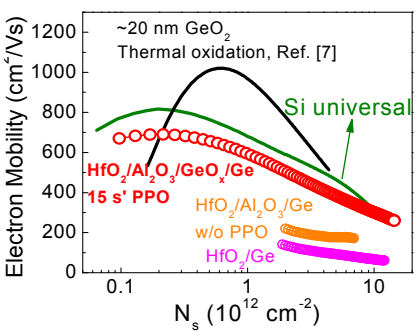

Fig. 4: Mobility of Ge nMOSFETs having different MOS interfaces.