28p-G2-14

Improvement of High N_s Mobility of Ge MOSFETs by Reducing GeO_x/Ge Interface Roughness

Rui Zhang, Po-Chin Huang, Ju-Chin Lin, Mitsuru Takenaka and Shinichi Takagi
The University of Tokyo, 2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-8656, Japan
Email: zhang@mosfet.t.u-tokyo.ac.jp

Introduction Ge MOSFETs are promising to overcome the performance of Si CMOS [1]. The high peak hole and electron mobility has been reported in Ge MOSFETs using plasma post oxidation Al_2O_3/GeO_x/Ge gate stacks [2, 3]. However, the high N_s mobility, which is important for MOSFETs operation, is still low in these Ge MOSFETs. It is confirmed that the surface roughness scattering is one of the dominant factors of mobility of Ge MOSFETs in high N_s region [2]. Therefore, improvement of the GeO_x/Ge interface flatness can be important for further enhancement of Ge MOSFETs performance. In this study, the impact of plasma post oxidation temperature on GeO_x/Ge interface roughness is examined. It is found that room temperature (RT) plasma post oxidation can realize an atomic flat GeO_x/Ge interface between Al_2O_3 and Ge, which provides record high mobility in the Ge p- and n-MOSFETs in the high N_s region.

Experiment SiO_2 field oxides were deposited on Ge (100) substrates by sputtering. The active areas were defined by etching the SiO_2. The source/drain regions were formed by ion implantation. Subsequent to the fabrication of 1-nm-thick Al_2O_3/Ge structures by ALD, the plasma post oxidation was carried out at 300 ^oC and RT to grow 1.2-nm-thick GeO_x/Ge interfaces. A 2^{nd}-ALD was performed to deposit 5 nm Al_2O_3, in order to suppress the gate leakage. PDA was performed at 400 ^oC for 30 min in N_2. TiN gate stacks were sputtered and patterned. Al contact pads were deposited for source/ drain and back electrodes.

Results and discussion Fig. 1 shows the cross section TEM images of Al_2O_3/GeO_x/Ge structures fabricated plasma post oxidation at 300 ^oC and RT. It is found that GeO_x/Ge interface roughness obviously reduces with a decrease of the oxidation time. The amount of the MOS interface flatness can also be evaluated from the oscillation of the amount of sub-oxides in the GeO_x/Ge interfaces using XPS measurements, as observed in SiO_2/Si interfaces [4]. It is confirmed that, during the RT plasma post oxidation, the GeO_x/Ge interface exhibits clear oscillations of Ge 1+ and 2+ components of the Ge sub-oxides with opposite phase to each other in a thickness period of ~0.3 nm (data not shown). These results indicate the formation of an atomic flat GeO_x/Ge interface by plasma post oxidation at RT, as explained by an atomic layer-by-layer growth mode similar to the SiO_2/Si interfaces.

The mobility of Ge p- and n-MOSFETs, shown in Fig. 2, was evaluated by split-CV method. It is found that the mobility of Ge p- and n-MOSFETs with the atomic flat GeO_x/Ge interface is enhanced by ~20% and ~25% in high N_s region for holes and electrons, respectively, against those of Ge MOSFETs with the GeO_x/Ge interfaces formed by plasma post oxidation at 300 ^oC. Compared with previous reports, the Ge p- and n-MOSFETs with the atomic flat GeO_x/Ge interfaces exhibit the record high effective mobility in high N_s region (Fig. 3 and 4). The mobility is also higher than the Si universal hole and electron mobility in both low and high N_s regions.

Conclusion It has been found that plasma post oxidation at RT realizes smoother GeO_x/Ge interfaces in an atomic level. By using this interface, record-high hole and electron mobility in Ge MOSFETs, which overcome the Si universal ones in both low and high N_s regions, have been demonstrated. This result is the first demonstration of the effective electron mobility in Ge nMOSFETs higher than the Si universal one in both low and high N_s regions.

Acknowledgement This work was supported by Grant-in-Aid for Scientific Research (No. 23246058) from MEXT of Japan.

References [1] S. Takagi et al., IEDM, 57 (2003). [2] R. Zhang et al., IEDM, 642 (2011). [3] R. Zhang et al., TED, 59, 335 (2012). [4] T. Hattori et al., APL 43, 470 (1983).

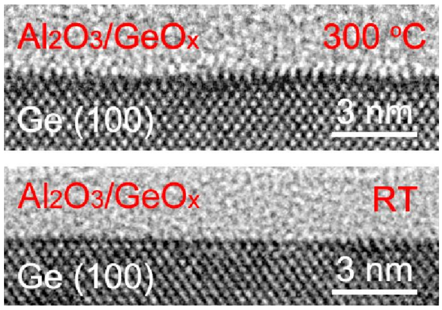

Fig. 1. TEM images of the Al_2O_3/GeO_x/Ge structures formed by 300 ^oC and RT plasma post oxidation.

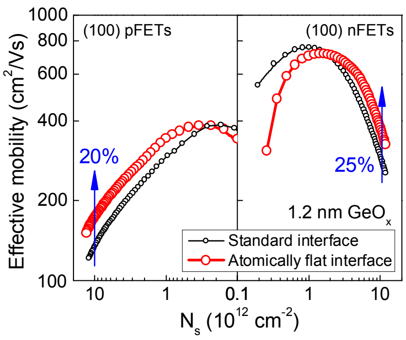

Fig. 2. The effective mobility of (100) Ge p- and n-FETs with 1.2-nm-thick standard and atomically flat GeO_x/Ge interfaces.

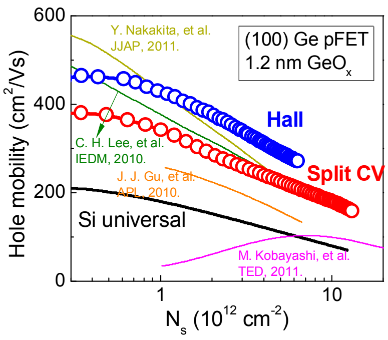

Fig. 3. The hole mobility of the Ge pFET with atomic flat GeO_x/Ge interface compared with those in previous reports.

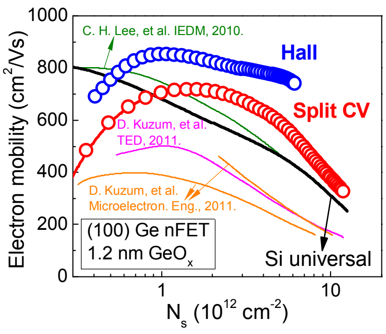

Fig. 4. The electron mobility of the Ge nFET with atomic flat GeO_x/Ge interface compared with those in previous reports.