Silicon carbide (SiC) is a fascinated wide band gap semiconductor for power MOS devices. Similarly to Si, SiO₂ film can be grown on SiC by conventional thermal oxidation. However, a small amount of carbon impurities and related defects at thermally grown SiO₂/SiC interfaces degrade channel mobility of SiC-MOSFETs. Furthermore, some studies on bias-temperature instability (BTI) of SiC MOSFETs exhibited both negative and positive threshold voltage shift due to trapped charges and/or mobile ions [1]. Recently, we have found that positively charged mobile ions are generated in SiO₂/SiC structures after post-oxidation annealing (POA) under diluted hydrogen ambient so called forming gas annealing (FGA) despite an improvement of interface property [2]. In this study, we investigated the impacts of FGA-induced mobile ions on interface properties.

SiC-MOS capacitors with thermal SiO₂ were fabricated on 4H-SiC(0001) substrates with an n-type epilayer. 40-nm-thick SiO₂ was formed by thermal oxidation in dry-O₂ ambient at 1100°C for 12 hours, followed by POA in Ar ambient at 1100°C for 1 hour. Then, FGA in 3% H₂/N₂ ambient was performed at 800°C for 30 min. At this step, positively charged mobile ions were self-generated in SiO₂. Then, Al gate electrodes and back contacts were deposited to fabricate SiC-MOS capacitors. In order to investigate relationships between the mobile ions and interface properties, the mobile ions were moved to gather at SiO₂/SiC or Al/SiO₂ interfaces by positive and negative bias-temperature stresses (PBTS & NBTS) at 200°C for 2 min, respectively.

Figure 1 shows bidirectional capacitance-voltage (C-V) curves for the fabricated capacitors measured at room temperature together with the ideal C-V curves. The flatband voltage of the ideal C-V curve was determined based on depletion capacitance [3]. The measured C-V curves exhibit stretch-out shape in the range from flatband to accumulation condition for both samples. Since fast traps which can respond to probe frequency (1 MHz) will contribute to additional capacitance, the positive shift of C-V curve with respect to an ideal one means the existence of slow traps near the conduction band edge. It should be note that the larger difference between the measured C-V curve and the ideal one in PBTS sample suggests the mobile ions at SiO₂/SiC interface may generate additional slow interface traps.

Figure 2 shows the energy distribution of interface state density (Dₛ) estimated by C−ψₛ method [3]. This method can precisely evaluate total amount of interface traps including very fast interface traps (>1 MHz). It is found that the Dₛ especially near the conduction band edge was decreased after NBTS. This means that the interface quality of FGA-treated SiC-MOS structures can be further improved by removing mobile ions from the SiO₂/SiC interfaces. However, an increase in Dₛ was observed for the PBTS sample. Therefore, it can be concluded that the FGA-induced mobile ions at SiO₂/SiC interfaces cause interface traps with various time constants.