Effect of Drain Voltage Dependent Subthreshold Voltage Reduction on Energy Efficiency in Steep Subthreshold Slope Transistors
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[Introduction] As the integration level of CMOS technology increases, not only high performance but also energy-efficient circuits are highly required. Steep subthreshold slope (S) transistors, such as I-MOS [1] and tunnel FET (TFET) [2], are promising for energy efficient VLSIs. It has been shown that the energy consumption (power-delay product) strongly depends on S and extremely low energy circuit operations can be achieved by steep S transistors [3]. However, some of TFETs show drain voltage dependent \( V_{th} \) reduction (so called DIBL), and the measured value of \( \eta = \frac{\Delta V_{th}}{\Delta V_{dd}} \) is as large as 0.74 below \( V_{dd} = 0.3V \) [4]. In this work, the dependences of energy consumption on S as well as \( \eta \) are investigated in subthreshold region below supply voltage \( (V_{dd}) \) of 0.3V. It is shown that \( \eta \) should be suppressed to achieve extremely low energy circuit operations using steep S transistors.

[Results and Discussion] When \( \eta \) is large (i.e. DIBL is worse), drain current never reaches on-current (\( I_{on} \)) at \( V_{dd} = V_{dd} \) in actual circuit operations. To consider the effect of \( \eta \), effective drain current (\( I_{eff} \)) is introduced [5]. \( I_{eff} \) is getting lower with larger \( \eta \) (worse DIBL) even at constant \( I_{on} \). Fig. 1 shows the calculated \( V_{dd} \) dependence of energy consumption at various S when \( \eta = 0 \) (no DIBL). \( I_{eff} \) is fixed to \( 1 \times 10^{12} \) A/\( \mu m \) at \( V_{dd} = V_{dd} \). Assuming logic circuits, the active time ratio (\( \xi \)) is set to be 0.001 [4]. Extremely low energy is also achieved in smaller S because steeper S shows higher \( I_{eff}/I_{on} \) ratio. The minimum energy is obtained around \( V_{dd} = 0.1V \) when S=30mV/dec. However, the energy consumption severely increases and the minimum energy also increases as shown in Fig. 2, where the \( \eta \) dependence of the energy consumption is shown at S=30mV/dec. This is because \( I_{eff} \) is degraded by the effect of \( \eta \) and the \( I_{eff}/I_{on} \) ratio decreases.

[Conclusion] Energy-efficient circuit cannot be realized in steep S transistors if \( \eta \) is large (DIBL is large). \( \eta \) should be suppressed to take advantage of steep S characteristics in steep S transistors.


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Fig. 1 Calculated \( V_{dd} \) dependence of energy at various S when \( \eta = 0 \). \( I_{eff} \) is fixed to \( 1 \times 10^{12} \) A/\( \mu m \) at \( V_{dd} = V_{dd} \).

Fig. 2 Calculated \( V_{dd} \) dependence of energy at S=30mV/dec at various \( \eta \). \( I_{eff} \) is fixed to \( 1 \times 10^{12} \) A/\( \mu m \) at \( V_{dd} = V_{dd} \).