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Effect of Drain Voltage Dependent Subthreshold Voltage Reduction on Energy Efficiency in Steep Subthreshold Slope Transistors

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[Introduction] As the integration level of CMOS technology increases, not only high performance but also energy-efficient circuits are highly required. Steep subthreshold slope (S) transistors, such as I-MOS [1] and tunnel FET (TFET) [2], are promising for energy efficient VLSIs. It has been shown that the energy consumption (power-delay product) strongly depends on S and extremely low energy circuit operations can be achieved by steep S transistors [3]. However, some of TFETs show drain voltage dependent V_{th} reduction (so called DIBL), and the measured value of η (= $|\Delta V_{th}/\Delta V_{ds}|$) is as large as 0.74 below V_{ds}=0.3V [4]. In this work, the dependences of energy consumption on S as well as η are investigated in subthreshold region below supply voltage (V_{dd}) of 0.3V. It is shown that η should be suppressed to achieve extremely low energy circuit operations using steep S transistors.

[Results and Discussion] When η is large (i.e. DIBL is worse), drain current never reaches on-current (I_{on}) at V_{gs}=V_{ds}=V_{dd} in actual circuit operations. To consider the effect of η, effective drain current (I_{eff}) is introduced [5]. I_{eff} is getting lower with larger η (worse DIBL) even at constant I_{on}. Fig. 1 shows the calculated V_{dd} dependence of energy consumption at various S when η=0 (no DIBL). I_{off} is fixed to 1×10^{12} A/μm at V_{ds}=V_{dd}. Assuming logic circuits, the active time ratio (ξ) is set to be 0.001 [4]. Extremely low energy is achieved in smaller S because steeper S shows higher I_{eff}/I_{off} ratio. The minimum energy is obtained around V_{dd}=0.1V when S=30mV/dec. However, the energy consumption severely increases and the minimum energy also increases as η increases as shown in Fig. 2, where the η dependence of the energy consumption is shown at S=30mV/dec. This is because I_{eff} is degraded by the effect of η and the I_{eff}/I_{off} ratio decreases.

[**Conclusion**] Energy-efficient circuit cannot be realized in steep S transistors if η is large (DIBL is large). η should be suppressed to take advantage of steep S characteristics in steep S transistors.

[Acknowledgement] This work was partly supported by Special Coordination Funds for Promoting Science and Technology from MEXT. **[Reference]** [1] K. Gopalakrishnan *et al.*, IEDM, p. 289, 2002. [2] W. Y. Choi *et al.*, IEEE EDL, vol. 28, p. 743, 2007. [3] H. Fuketa *et al.*, IEDM, p. 559, 2011. [4] K. Tomioka *et al.*, VLSI Tech. Symp., p. 47, 2012. [5] M. H. Na *et al.*, IEDM, p. 121, 2002.

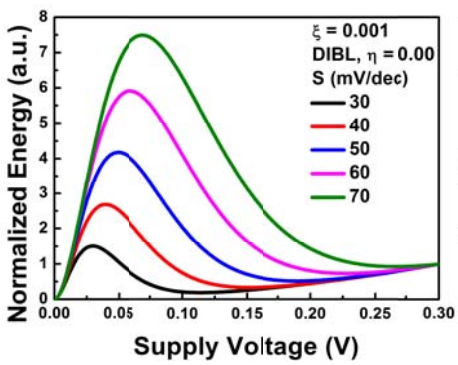

Fig. 1 Calculated V_{dd} dependence of energy at various S when η=0. I_{off} is fixed to 1×10^{12} A/μm at V_{ds}=V_{dd}.

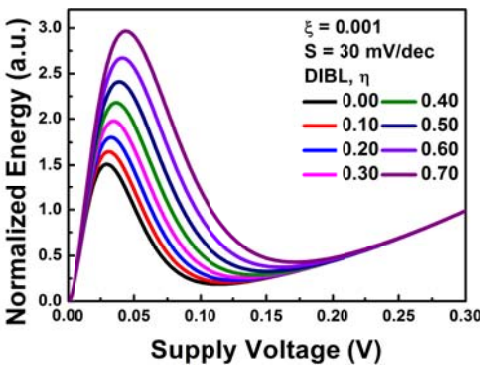

Fig. 2 Calculated V_{dd} dependence of energy at S=30mV/dec at various η. I_{off} is fixed to 1×10^{12} A/μm at V_{ds}=V_{dd}.

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