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Trapping and Detrapping of Carriers by Individual Dopants in Lateral Nanoscale *p-n* Junctions

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Introduction

Nanoscale *p-n* junctions are important building blocks for future nanoelectronics. Previously, we studied the effects of light illumination on lateral nanowire *p-n* junctions and we reported the observation of photon-induced random telegraph signals (RTS).[1] RTS was found to be due to potential fluctuations due to trapping and detrapping of photogenerated carriers within a phosphorus-boron (P-B) pair. In the present work, we observed RTS in lateral nanoscale *p-n* junctions even in dark conditions, at temperatures below 30 K. These current fluctuations are ascribed to charge trapping by an individual dopant located in the depletion region of the device.

Device structure and measurement setup

We fabricated nanoscale lateral *p-n* junction diodes in thin silicon-on-insulator (SOI) layer ($t_{Si} \cong 10$ nm). Figure 1 shows schematically the device structure and *I-V* measurement setup. The nanowire length and width are 1000 nm and 150 nm, respectively. The *n*-type region was doped with phosphorus ($N_D \approx 1.0 \times 10^{18}$ cm^{-3}), while the *p*-type region was doped with boron ($N_A \approx 1.5 \times 10^{18}$ cm^{-3}). A co-doped region, doped with both P and B, is designed in the center of the nanowire. The *p*-type region is positively biased for these measurements, i.e., the *p-n* junction is forward-biased, while the *n*-type region and substrate are grounded.

Experimental results and discussion

In this study, we measured *I-V* characteristics in dark conditions, at various temperatures below 100 K, as shown in Fig. 2. The data for room temperature (T = 300 K) is also shown for reference. We observed that the voltage for current onset is increased by decreasing temperature. This is caused by the dopant freeze-out effect,[2,3] which triggers the reduction of carrier concentration and an increase in the parasitic resistances of the leads at lower temperatures.

At temperatures below 30 K, current fluctuations are also observed and can be ascribed to charge trapping and detrapping. For each temperature, the time dependence of the current was measured as a function of applied bias, as shown in the examples in Fig. 3 at T = 6 K. Random telegraph signals (RTS) with two levels were observed, suggesting that the trap is most likely a single dopant. The RTS becomes noticeable and its frequency is increased by increasing the forward bias, indicating that the RTS (trapping and detrapping) is sensitive to the change of electric field near the *p-n* junction. Therefore, a single dopant located in the depletion region may be responsible for the RTS.

These results indicate that individual dopants have important impact on the electrical characteristics of nanoscale *p-n* junctions, allowing the development of single-dopant devices using the *p-n* junction structure.

References [1]A. Udhiarto, *et al.*, Appl. Phys. Express **5**, 112201 (2012). [2]S. M. Sze, *Physics of Semiconductor Devices*, 2nd Ed., Wiley, p. 26 (1981). [3]D. Foty, Cryogenics **30**, 1056 (1990).

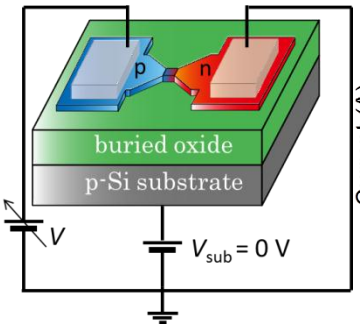

Fig. 1. Schematic structure of nanoscale lateral *p-n* junctions and *I-V* measurement setup.

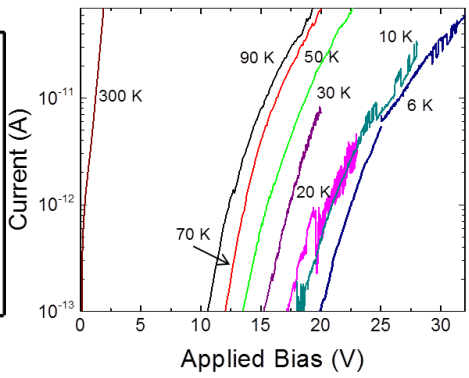

Fig. 2. *I-V* characteristics in forward bias at different temperature (T = 300 K and T < 100 K). For T < 30 K, current fluctuations can be observed.

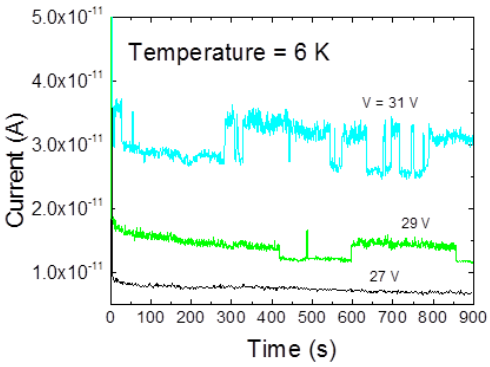

Fig. 3. Examples of *I*-time characteristics at T = 6 K for different applied biases. Two-level RTS can be seen above a certain forward bias.