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Ge/Si Hetero-Junction TFETs with In-situ Boron-Doped Ge-Source

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1. Introduction A Ge/Si hetero-structure with staggered type-II band alignment can effectively reduce tunneling width in the source junction, which can simultaneously satisfy the high on/off current ratio and steep SS in the TFET operation [1]. In the Ge/Si hetero TFETs, tunneling currents are generated near the Ge/Si junction and, therefore, a formation of high quality Ge with abrupt doping profile and high doping concentration in Ge are important [2]. Ion implantation for doping in Ge layers can cause generation of many defects in the Ge layers. Moreover, the formation of the abrupt Ge/Si hetero-structure is very difficult because Ge atoms can diffuse into Si during high temperature activation annealing. In this study, Ge/Si hetero-junction TFETs are demonstrated by using epitaxial Ge-source layers with in-situ boron doping by molecular beam epitaxy at extremely low temperature of 200 °C.

2. Experiment Commercial silicon-on-insulator substrates are used for starting materials. Phosphorus ion implantation is used for drain formation with low acceleration energy of 3 keV, followed by RTA at 900 °C for activation. 25-nm-thick Ge layers are grown by molecular beam epitaxy with/without in-situ boron doping (Ge:B/Ge) at 200 °C. First 13 cycles Al_2O_3 layers are deposited by atomic layer deposition, followed by electron cyclotron resonance plasma post oxidation is performed to ensure the high quality MOS interface between Al_2O_3 and Ge [3]. Second 20 cycles Al_2O_3 layers are deposited by atomic layer deposition, followed by post deposition annealing is carried out at 400 °C in nitrogen ambient for 30 min. Ta is deposited as the gate metal, followed by Ni and Al deposition for the source contact and the contact pad, respectively. Post metallization annealing is carried out at 400 °C in nitrogen ambient for 30 min.

3. Results and Discussion Fig. 1 shows I_D-V_G characteristics of fabricated Ge(B)/SOI TFETs and Fig. 2 shows subthreshold swing (SS) of Ge(B)/SOI TFETs extracted from Fig. 1. The device performance improvement including 4-times-higher drain current is obtained by increasing the boron concentration from 10^{16} cm^{-3} to 10^{20} cm^{-3}. Under the optimum boron concentration of 10^{20} cm^{-3}, the large drain on/off current ratio over 6 orders of magnitude and steep subthreshold swing of 58 mV/dec are obtained.

4. Conclusions High performance TFETs are demonstrated by using hetero-junction of highly in-situ boron doped Ge and silicon.

References [1] S. Kim et al., Symp. VLSI Tech. Digest (2009) 178. [2] D. Leonelli et al., ESSDERC (2010) 170.
[3] R. Zhang et al., Appl. Phys. Lett., 98, (2011) 112902.

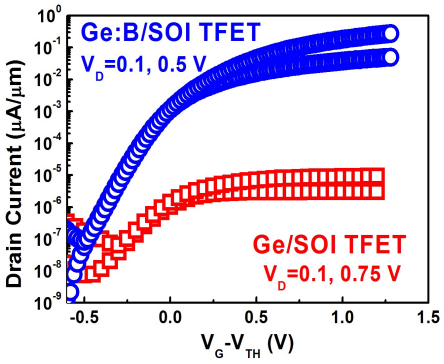

Fig. 1 I_D-V_G characteristics of Ge(B)/SOI TFETs L/W=20/50 μm.

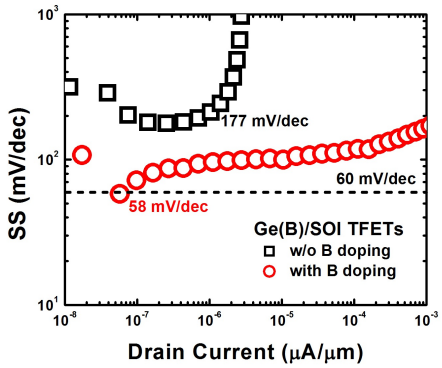

Fig. 2 Subthreshold swing of Ge(B)/SOI TFETs extracted from Fig 1.

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