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An Improved Self-Aligned Ohmic-Contact Process for Graphene-Channel Field-Effect Transistors

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1. Introduction

Graphene is a layer of pure carbon atoms arranged in hexagonal honeycomb lattice. Being two-dimensional material has made graphene a superior electrical conductor which makes it one of the most attracted candidates for the new transistor channel material. However, the full applications of graphene are still limited by some critical issues such as low on/off current ratios and low cut-off frequencies despite of its outstanding intrinsic carrier transport properties [1]. Our current research focuses on improving the speed/drivability performances of Graphene-channel Field-Effect Transistors (GFETs). The fabrication of high-performance GFETs is challenging because the parasitic resistance in an extrinsic regions significantly degrade the GFET performance.

2. Experimental method and result

The graphene coating and baking with ultraviolet light sensitive polymer films (photoresist) during device fabrication is well known to contaminate, thus degrading the intrinsic properties of graphene. In this study, we first report on Al sacrificial layer [2] to prevent the photoresist from directly contacting with graphene in an ohmic contact area, which spectacularly reducing the source/drain ohmic contact resistance from 9300 to 1650 Ω μm for a CVD-grown graphene transferred onto a SiO_2/Si substrate (see Fig. 1), which is a contact resistance comparable to the state-of-the art ones [3-5]. Second, we introduce a self-aligned source-drain technique [6] with the aforementioned Al sacrificial layer as the ohmic protection that can minimize both the extrinsic access resistance and the damage to the intrinsic graphene electrical property (see Fig. 2).

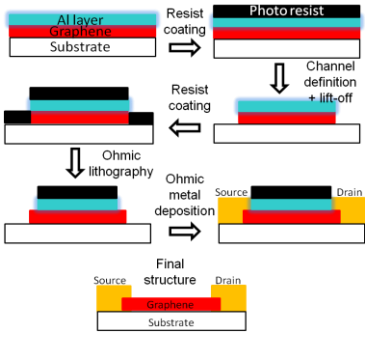

Fig.2 Basic process flow of the graphene-metal ohmic contact formation with an Al sacrificial layer.

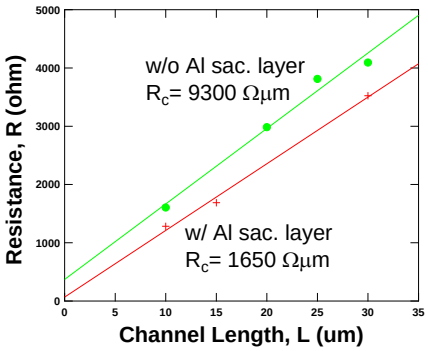

Fig.2 Obvious contact resistance difference (Rc) of the graphene-metal ohmic contact with and without an Al sacrificial layer.

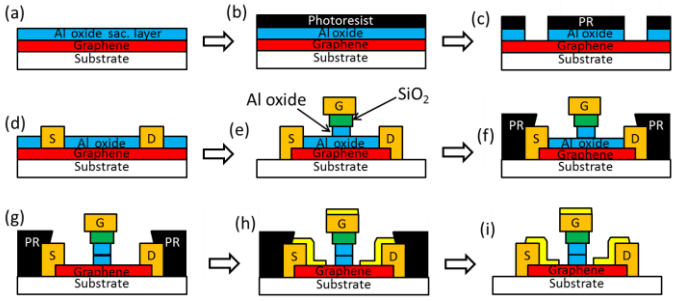

Fig. 3 Process flow of the self-aligned source-drain formation with an Al sacrificial layer.

3. Conclusions

The process technologies proposed here will be able to assure the GFET performance projections beyond the level of any existing FETs using conventional semiconductor materials.

Acknowledgements

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