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InAlAs キャップを用いた III-V CMOS フォトニクス•プラットフォーム上導波路型 InGaAs フォトディテクタの暗電流低減

Dark current reduction of waveguide InGaAs MSM photodetector on III-V CMOS photonics platform by InAlAs cap layer

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1. Background

To solve the metal electronic interconnect problem by optical interconnect, silicon photonics is promising and is the main stream due to the natural compatibility with micro-electronics CMOS process lines [1]; but laser problem still remains for silicon photonics. Though the III-V/Si hybrid platform [2] can solve the laser problem, it seems difficult to integrate monolithically III-V/Si hybrid photonics and Si CMOS electronics due to the thermal budget difference between III-V and Si.

To realize the real monolithic integration for electronics and photonics, we develop a unique platform called 'III-V CMOS photonics platform' which uses III-V-OI wafers by direct wafer bonding to fabricate high-performance electronics and photonics devices [3]. On this platform, sharp bends [4], AWGs [4], grating couplers [5], modulators/switches [6], MOSFETs [7] have been demonstrated so far. In addition, we have demonstrated the waveguide InGaAs MSM PDs [8]. However the demonstrated PD exhibited relatively large dark current. Thereby, in this paper, we introduce an InP/InAlAs layer as Schottky barrier enhancement (SBE) layer between the InGaAs absorption layer and metal electrode to reduce the dark current.

2. Fabrication

For device fabrication, we prepare III-V-OI wafers by direct wafer bonding. At first, i-InP/i-InGaAs/i-InAlAs/i-InP are grown on an InP wafer. A 2.3μm-thick SiO_2 BOX layer is also thermally grown on a Si wafer. After depositing Al_2O_3 on both wafers by atomic layer deposition (ALD), the two wafers are bonded together. Finally, the InP/InAlAs/InGaAs/InP on SiO_2/Si wafer is obtained by etching the InP substrate.

By the III-V-OI wafers, we fabricate the waveguide InGaAs MSM PD as shown in Fig. 1. At first, we form InP photonic-wire waveguides and InGaAs mesas by deep-ultra-violet (DUV) lithography and reactive ion etching (RIE). Then, we etch the InP/InAlAs/InGaAs on top of the InP waveguides. We deposit Al_2O_3 for passivation by ALD and open a contact window on InGaAs mesa. Finally, we form the interdigitated electrodes by Ni deposition and lift-off.

3. Experimental results

As the Fig. 2 shows, the dark current of the PD can be decreased to 7 nA at 1V bias after the SBE layer insertion onto the InGaAs layer, which has a 2-order reduction in comparison with the first demonstration. When 2 V bias is applied, we obtain the photocurrent of 32 μA. By taking into account of 8-dB coupling loss, the intrinsic responsivity is estimated to approximately 0.2 A/W. The SBE layer may also block some photo-generated carriers, resulting in relatively low responsivity, which can be improved by the gradually changed SBE layer.

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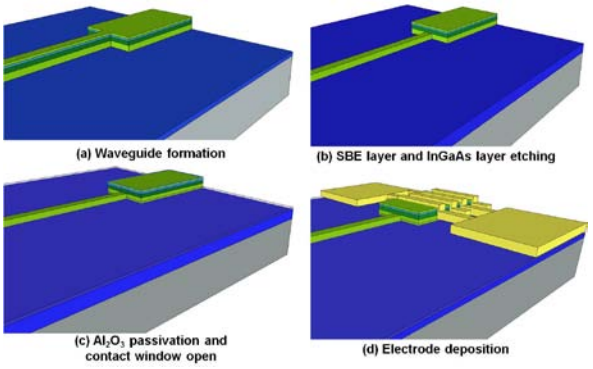

Fig. 1 Process flow for waveguide InGaAs PD.

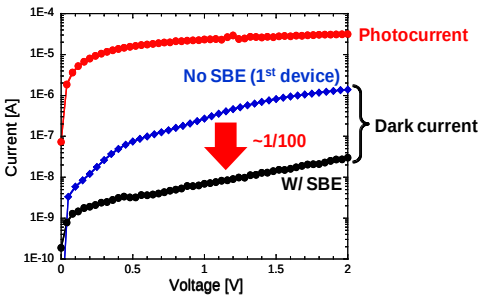

Fig. 2 Dark and photon current of the PD.