17p-S1-2

Energy gap formation and gap states analysis in bilayer graphene under the ultra-high displacement

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Our goal is to exploit the extremely high potential of graphene toward the transistor application. The ability to electrostatically tune the band gap in bilayer graphene attracts great attention. Although the band gap of ~250meV is predicted, $I_{on/off}$ is considerably small at room temperature (only ~100). This is explained by the variable range hopping in gap states. Here, if we recall that the interface states for SiO_2/Si result from the dangling bonds of Si (P_b center), this kind of interface states are not expected for graphene due to no dangling bonds on the basal plane. The origin for the gap states is still open question. However, the research on gap states is quite limited due to the unreliable quality of the high-k top gate insulator on bilayer graphene.

Recently, we demonstrate the ultra-high displacement of ~8 V/nm (n=~4×10^{13} cm^{-2}) in bilayer graphene using the solid state Y_2O_3 top gate [1], which has been reached only by the ion gating so far. This provides the access to the carrier response issue in the largely-opened band gap. In this study, we focus on the quantum capacitance (C_Q) measurements for bilayer graphene because the density of states (DOS) can be extracted through $C_Q=e^2$DOS and the scattering issues can be excluded in the C-V measurement. The frequency dispersion in C-V curve reveals that the carriers in bilayer graphene electrically communicate with trap sites within the band gap.

Two possible origins are proposed; one is the external origin that the carriers in graphene electrically communicate with trap sites “in oxides”. This is categorized as border trap. The other is the internal origin, that is, gap states created in bilayer graphene due to the local breakdown of A-B stacking. The A-B stack breaking means the stack of two monolayers, resulting in the local conduction path. Here, the former is more time-consuming process than the later. The local conduction sites formed by the breakdown of A-B stacking might be more probable because the frequency dispersion in C-V curve at the band gap region does not saturate even at 1 MHz.

Generally, it is difficult to control the band gap precisely for very thin Si (SOI) transistor (a few nm) due to the thickness variation. Although it was expected that the physical properties, i.e. band gap, are fixed just by selecting the layer number for graphene system, the above-discussion suggests that it is important to precisely control the circumstances of graphene, such as atomically flat substrate.

[1] K. Kanayama, K. Nagashio, T. Nishimura, and A. Toriumi, APL, 2014, **104**, 083519.
[2] K. Nagashio, K. Kanayama, T. Nishimura, and A. Toriumi, IEDM Tech. 2013, 503.