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Dependence of dielectric constants, leakage currents, and ferroelectric hystereses on $Hf_{0.5}Zr_{0.5}O_2$ thicknesses in MIM Capacitors

Nanoelectronics Research Institute, AIST, Japan

S. Migita, H. Ota, Y. Morita, and M. Masahara

E-mail: s-migita@aist.go.jp

1. Introduction

Ferroelectricity is attractive for the functionalization of electronic devices. It is valuable not only for memory applications, but also for logic devices that materialize a steep subthreshold slope [1]. Existence of ferroelectric property in metastable HfO_2–based systems has been recently reported and widely investigated [2-6]. These HfO_2-based systems are friendly with CMOS process because they are free from lead and bismuth. Ferroelectric properties in these systems are closely correlated with the chemical composition of metal elements [3, 5] and film thicknesses [6]. One of the key processes is the capped-annealing (Cap-PDA) that promotes formation of metastable crystalline phases in HfO_2 systems [7]. In this work, focusing on $Hf_{0.5}Zr_{0.5}O_2$ films, we examined the impact of film thickness on dielectric constant, leakage current, and ferroelectric switching systematically.

2. Experimental

Metal-insulator-metal (MIM) capacitors, consist of TiN bottom electrode (40 nm), $Hf_{0.5}Zr_{0.5}O_2$ dielectric films, and TiN top electrodes (40 nm), were fabricated by sputtering these films in series on Si substrates. Chemical composition of hafnium and zirconium was adjusted by an alternating sputtering of HfO_2 and ZrO_2 targets in a short period less within 1 nm thickness deposition. Thicknesses of $Hf_{0.5}Zr_{0.5}O_2$ films were between 5.3 nm and 31.8nm. Following to the crystallization anneal by the Cap-PDA at 600°C for 20s in 100 Pa N_2 condition, capacitors (100 um x 100 um) were fabricated by lithography and dry etching. C-V and J-V characteristics were measured using the LCR meter (Agilent 4284A) and the semiconductor parameter analyzer (Agilent 4156C) at room temperature.

3. Results and Discussion

C-V and J-V characteristics of MIM capacitors are shown in **Fig. 1**. Depending on the film thickness, the capacitance and the leakage current decrease naturally. Hysteresis of C-V loop caused by ferroelectric switching is remarkable in 8.0 and 10.6 nm thicknesses.

Impacts of film thicknesses on electrical properties are summarized. Except for the thinnest case (5.3 nm), the dielectric constant is large for the thinner films and decreases gradually in accord with the film thickness (**Fig. 1(c)**). The failure of 5.3 nm-film case seems to be correlated with the drastic increment of leakage current (**Fig. 1(d)**).

The ferroelectric switching charge Q_F was calculated by the integration of hysteresis loop in the C-V curve and averaged between the positive and negative bias region (**Fig. 1(e)**). It is clear that the magnitude of ferroelectric property is large for thinner films, and correlated with the enhancement of the dielectric constant. It is probable that emergence of ferroelectricty in $Hf_{0.5}Zr_{0.5}O_2$ films is strongly affected by the interface.

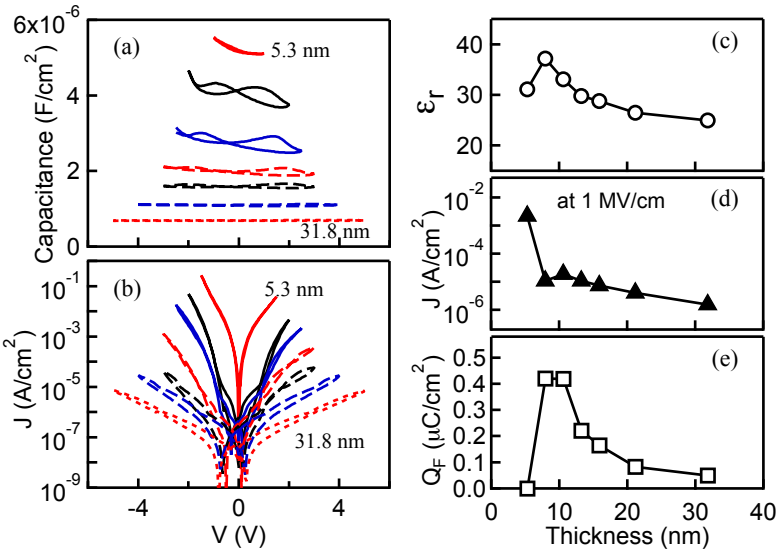

Fig. 1 (a) C-V and (b) J-V characteristics of TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN capacitors with 5.3, 8.0, 10.6, 13.3, 15.9, 21.2, and 31.8 nm thicknesses, prepared by Cap-PDA at 600°C. Summary of thickness dependences of (c) dielectric constants (at 0 V), (d) leakage currents (at 1 MV/cm), and (e) ferroelectric switching charges.

4. Conclusions

Ferroelectric behavior of $Hf_{0.5}Zr_{0.5}O_2$ films is enhanced at thinner film region less than 20 nm. It suggests that the interface between $Hf_{0.5}Zr_{0.5}O_2$ films and metal electrode has a crucial role for the formation of ferroelectric phase. In order to attain ferroelectricity in ultrathin films, it is mandatory to control the leakage current.

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References [1] S. Salahuddin and S. Datta, Nano Lett. **8**, 405 (2008). [2] T. S. Böscke *et al.*, Appl. Phys. Lett. **99**, 102903 (2011); Appl. Phys. Lett. **99**, 112904 (2011). IEDM 2011, p. 547. [3] J. Müller *et al.*, Appl. Phys. Lett. **99**, 112901 (2011); J. Appl. Phys. 110, 114113 (2011); Nano Lett. **12**, 4318 (2012); IEEE EDL 33, 185 (2012); VLSI 2012 p. 25; IEDM 2013, p. 280. [4] S. Müller *et al.*, IEEE EDL **33**, 1300 (2012). [5] T. Olsen *et al.*, Appl. Phys. Lett. **101**, 082905 (2012). [6] M. H. Park *et al.*, Appl. Phys. Lett. **102**, 242905 (2013). [7] S. Migita *et al.,* VLSI Tech. 2008, p. 152.