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Analysis of Delay Time Degradation of Ultra-Low Supply Voltage CMOS Circuit Operating in Subthreshold Region

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[Introduction] Recently, batteryless systems have attracted much attention [1]. Since the harvested energy is generally very small, the energy consumption should be extremely reduced. The subthreshold circuit is one of the solutions because the most effective way to reduce power is V_{dd} scaling [2,3]. However, the circuit speed is severely degraded in the subthreshold region due to small on-current (I_{on}). Furthermore, the subthreshold circuits may be very sensitive to the change in various device and circuit parameters. In the previous work [4], we have shown that measured drain current of FETs is severely degraded in the subthreshold region in the presence of DIBL, which also degrades the circuit performance. It is essential to clarify the origins of the performance degradation in order to design ultra-low energy subthreshold circuits.
[Results and Discussion] In order to investigate the effect of DIBL on CMOS circuits, five sets of nFETs and pFETs (A–E) with different DIBL were assumed. Fig. 1 shows simulated delay time of CMOS ring oscillators which are composed of the five sets of nFETs and pFETs (A–E). The delay is normalized to that of A. The largest DIBL device (E) shows the slowest delay time. Moreover, as V_{dd} is scaled down into subthreshold region, the delay becomes more sensitive to DIBL and the delay increment ratio drastically increases. To find the reasons of delay degradation due to DIBL, the trajectory of the operation points in nFET is simulated. Fig. 2 (a) and (b) compare I_{ds}-V_{ds} curves and the trajectories with various DIBL at V_{dd} of 1.2 V. Although the peak trajectory current (I_{peak}) decreases by DIBL [5], the DIBL dependence is small. On the other hand, the current decreases by DIBL and corresponding I_{peak} is very sensitive to DIBL and is severely degraded at 0.3 V as shown in Fig. 3 (a) and (b). Therefore, the origin of the delay degradation in subthreshold circuit is the reduction of transient current caused by DIBL. Figs. 2 and 3 also show the trajectories with C_{load} and Fig. 4 shows normalized I_{peak} with various C_{load}. The effect of DIBL on normalized I_{peak} is independent of C_{load}, indicating that the delay is primarily determined by I_{peak}. [**Conclusion**] The effects of DIBL on circuits speed in subthreshold circuits are investigated. It is found that the delay is degraded more sensitively by DIBL in subthreshold circuits because the I_{peak} decreases due to DIBL, indicating that DIBL should be suppressed for subthreshold circuits applications.

[References] [1] D. Buss, IEDM, p.239, 2011. [2] T. Sakurai, IEICE Trans. Electron., p. 429, 2004. [3] H. Fuketa et al., IEDM, p. 559, 2011. [4] S.-M. Jung et al., JSAP autumn meeting, 2013. [5] M. H. Na et al., IEDM, p. 121, 2002.

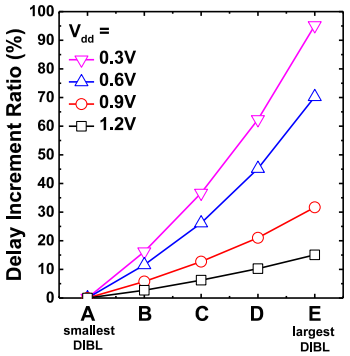

Fig. 1 Normalized delay of CMOS ring oscillators with various DIBL (A–E) at V_{dd} of 0.3 V, 0.6 V, 0.9 V, and 1.2 V.

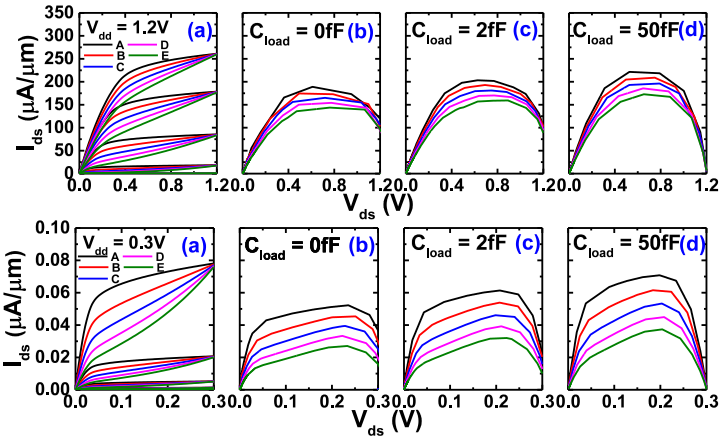

Fig. 2 (upper) and 3 (lower) (a) Simulated output curves of nFETs and trajectory curves with (b) C_{load} = 0 fF, (c) 2 fF, and (d) 50 fF during switching at V_{dd} of 1.2 V(upper) and 0.3 V (lower).

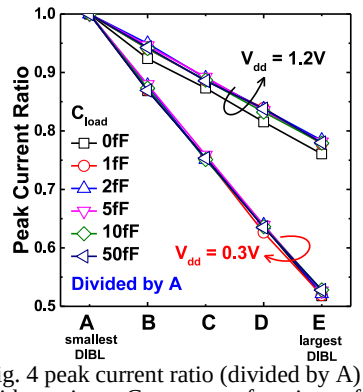

Fig. 4 peak current ratio (divided by A) with various C_{load} as a function of DIBL at V_{dd} of 1.2 V and 0.3 V