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酸化濃縮後の追加酸化による薄膜化が GOI 薄膜の特性に与える影響

Effects of thinning condensation UTB GOI films by additional thermal oxidation on GOI Characteristics

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【**Background**】The fundamental limits of Si as MOS channel materials strongly demand new channel materials with higher mobility, such as Ge or III-V chemical compounds [1]. Especially, Ge is regarded as one of the most promising materials because of its characteristics of both high hole and elecrtron mobility and easy introduction into the Si platform. Moreover, a UTB (Ultra-thin body) GOI (Ge-On Insulator) structure is very important to suppress the short channel effect. Here, Ge condensation method [2, 3] is one of the most promising techiniques to fabricate UTB GOIs. Judging from the technology nodes into which the Ge channel is intorduced, not only the demonstration of UTB GOI MOSFETs but also the understanding of the physical and electrical characteristics GOI channels less than 10 nm are quite important. In this study, we have analysed the characterisitics of GOI layers with the thickness of 11 nm, 9.6 nm, and 6.7 nm formed by additional oxidation of Ge condensation GOI layers. Also, we have successfully demostrated the operation of GOI pMOSFETs with thickness of 6.7 nm.

【**Experimnetal**】Fig. 1 shows the process flow of the present UTB GOI layers, including the Ge condensation. The Ge condensatoin process was performed with changing the oxidation temperatures from 1100 °C, 1050 °C, 1000 °C, 950 °C to 900 °C. After each oxdiation step, intermixing annealing was performed in N_2 at 1050 °C, 1000 °C and 950 °C. After fabricating 100% GOI, additional oxidation was carried out at 900 °C for 10, 30, and 50 minutes to form thinner GOI layers. As a result, the GOI thickness of 11, 9.5, and 6.7 nm was acheived. Ni was deposited for S/D contact and Al was deposited for back contact. The device operation was examined under the back gate confirguration. Also, the Hall measurement was used to measure the hole concentration of each GOI layer.

【**Results**】Fig. 2 shows the hole concentraions of the as-condensed (14.5 nm) and thinned GOI layers. We can clearly see that the hole concentration increases after the additional oxidation. Comparing with hole concentraion of 2.17×10^{17} cm^{-3} in the initial GOI layer, fabricated by the optimized Ge condensation process [4], the hole concentraion of the GOI layers after additional oxidation for 10, 30 and 50 minutes resulted in 4.8 x 10^{17}, 2.8 x 10^{18} and 7.9 x 10^{18} cm^{-3}, respctively. This increase in the hole concetration is attbituble to any defect generation during the additional oxidation at high temperature oxidation. Fig. 3 shows the I_d-V_g curve of the pMOSFETs with the different GOI thickness. Since the MOSFETs operate under the accumulation mode, V_{th} of the I_d-V_g curve was shifted to positive direction with an increase in the hole concentration. Fig. 4 shows the effective hole mobility of GOI pMOSFETs. As the GOI thickness becomes thinner, the mobility is degraded. In particular, larger degration in the low N_s region can be explained by the increase in Coloumb scattering due to higher hole concentration in the thinner body. Moreover, the lowering in the mobility for the 6.7-nm-thick GOI in high N_s region could be caused by surface roughness scattering.

【**Conclusion**】In this study, we have thinned GOI layer to thickness under 10 nm by additional oxidation in Ge condensation process. Moreover, we have analyzed the incresement in hole concentration on thinned GOI layers. We have also demonstrated GOI pMOSFETs with thickness of 6.7 nm.

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【**Reference**】[1] S. Takagi *et al.*, SSE **51.** 526 (2007) [2] S. Nakaharai *et al.*, APL **83**, 3561 (2003) [3] K. Ikeda *et al.*, SSDM, 32 (2008) [4] W.-K. Kim et al., SSDM, 774 (2013)

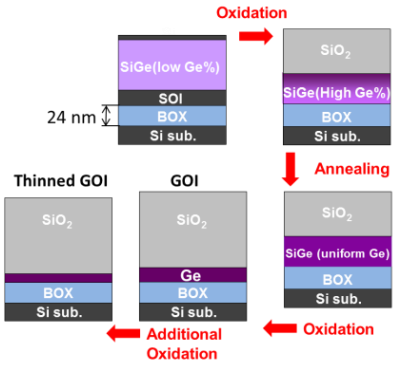

Fig. 1 Process flow of Ge condensation. The thickness of GOI layers were 11 nm, 9.6 nm, and 6.7 nm

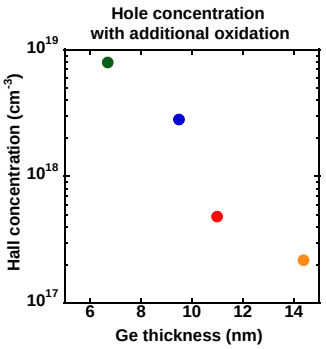

Fig. **2** Hole concentration of GOI layers with additional oxidation

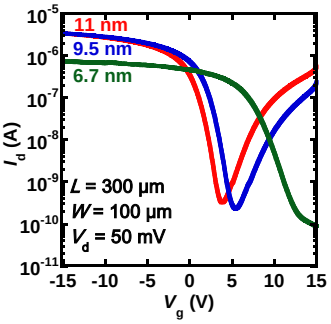

Fig. 3 I_d-V_g curves of GOI p MOSFETs

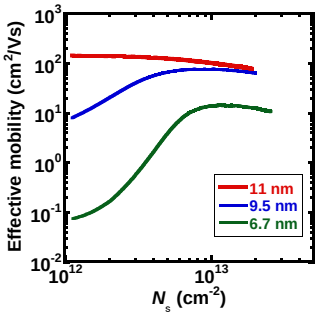

Fig. 4 Effective hole mobility as a function of N_s in GOI pMOSFETs