18p-A18-14

Ge-on-Insulator Fabrication by Smartcut Technology for Ge CMOS Photonics Platform

Jian Kang[1,2], Xiao Yu[1,2], Mitsuru Takenaka[1,2], and Shinichi Takagi[1,2]
[1]The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-8656, Japan, [2]JST-CREST
E-mail: linick@mosfet.t.u-tokyo.ac.jp

Introduction

Recently, bottlenecks in bandwidth and power consumption of traditional electrical interconnection severely limit the growing functionalities in data processing. Electronic-photonic integrated circuits (EPICs) provides a good solution for optical interconnects with large data capacity and low power [1]. Ge has been demonstrated to be a most promising material in both electronic and photonic application meanwhile being compatible with the mainstream CMOS technologies [2]. In this paper, we propose a concept of Ge CMOS photonics platform on which high-performance Ge CMOS transistors and Ge-based photonic-wire devices can be monolithically integrated as shown in Fig. 1. For Ge CMOS photonics platform, we have fabricated high-quality Ge-on-Insulator (GOI) wafers by wafer bonding and Smartcut technology.

Fabrication procedure

The fabrication process and structure of the GOI wafer are shown in Fig. 2. First 100 nm SiO_2 was deposited on a 2-inch bulk Ge (100) donor wafer to protect its surface, on which H^+ ion was implanted with dose of 4×10^{16} cm^{-2} under 80 keV [3]. After removing the SiO_2 capping layer, GeO_x passivation [4] was performed to form $Al_2O_3/GeO_x/Ge$ structure on the implanted Ge surface, which is supposed to improve the back interface property of the GOI substrate. Then the Ge donor wafer is manually bonded with a Si handle wafer. We formed 2-μm thick SiO_2 BOX layer by thermal oxidation, which is necessary for strong optical confinement in Ge photonic-wire waveguides. The bonded wafer is then annealed in vacuum at 300 °C for 30 min to enhance the bonding strength, followed by a 2nd annealing in which the temperature is generally raised up to 400 °C to induce the splitting of Ge wafer. Finally, CMP by alkali colloidal silica suspension is performed to reduce the surface roughness of the GOI substrate.

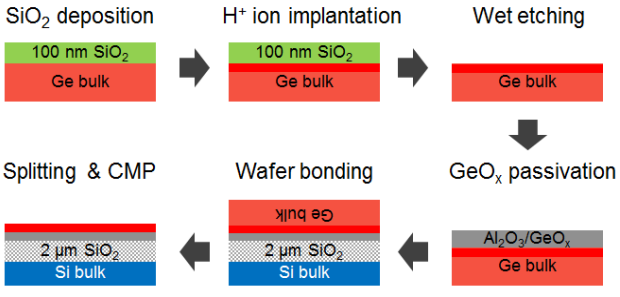

Fig. 2 Fabrication process and structure of GOI substrate

Results and discussion

In order to characterize the GOI quality, a Hall device has been fabricated using the GOI substrate. Figure 3 shows the Hall measurement result of the Hall device with a Ge layer thickness of 400 nm. It is found that the majority carrier of fabricated GOI substrate is hole, with Hall mobility of 916 cm^2/Vs and the carrier density of 5.4×10^{15} cm^{-3}. The low impurity concentration and acceptable Hall mobility indicates a good Ge layer quality in the GOI substrate, which is mandatory to the EPICs application.

Acknowledgement

This work was partly supported by New Energy and Industrial Technology Development Organization (NEDO) and MEXT Grant-in-Aid for Scientific Research(S).

References

[1] M.S. Dahlem, et al., *General Assembly and Scientific Symposium* (2011) [2] J.F. Liu, et al., *ESC Trans.* **16**, issue 10 (2008) [3] L. Chen, et al., *Opt. Express*, **16**, 11513 (2008) [4] R. Zhang et al., *Appl. Phys. Lett.* **98**, 112902 (2011)

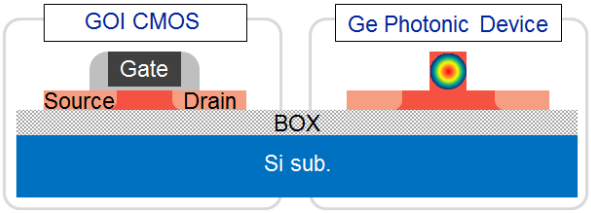

Fig. 1 Concept of Ge CMOS photonics platform

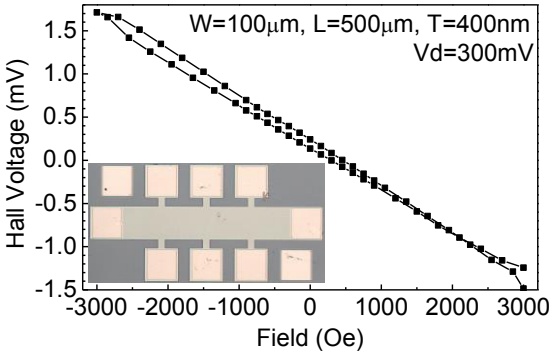

Fig. 3 Hall measurement results, the inset shows top view of the Hall device