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STT-MRAM および不揮発性ロジックの現状と将来展望

Technology of STT-MRAM and Nonvolatile Logic, and its Potential

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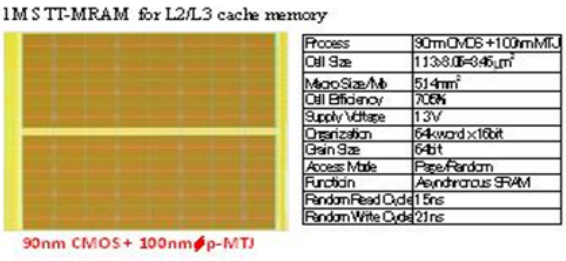
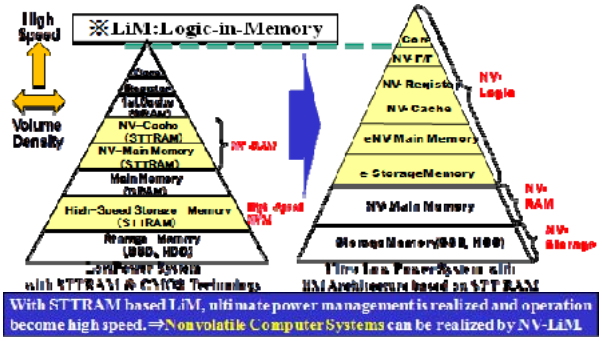
In this invited review talk, the directionality of the revolution of the semiconductor memory hierarchy structure in the future from the background mentioned above is discussed. The impact of STT-MRAM is introduced. Especially, it is discussed that fine-grained power gating technique plays a key role in designing low-power and high-performance STT-MRAMs. Comparison of memories using several type STT-MRAM cells with SRAM cell is given. It is shown that the 64B access in 32MB STT-MRAM consumes about 95% smaller write power than SRAM counterpart in 90nm technology node.

Finally, from the viewpoint of the super-low power consumption system in the future, it is discussed the effect to the logic of nonvolatile RAM by introduces Nonvolatile Logic that fuses the STTRAM with semiconductor CMOS logic.



1.5nsec/2.1nsec Random Read/Write Cycle 1Mb STT-RAM



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