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Analysis of Heat Escape Paths in FinFETs Using Phonon Monte Carlo Simulation

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Introduction: The heat conduction property is one of the main concerns for nanoscale FETs relating to reliability and performance [1,2]. We have recently developed Monte Carlo (MC) simulator for solving the phonon's Boltzmann transport equation taking account of rigorous physical models [3]. In this study, we present in-depth analysis about the heat conduction properties in nanoscale FinFET structure based on the various simulation techniques (MC, a finite element method, and an equivalent thermal circuit model) [4].

Simulation Method and Results: Fig. 1 schematically illustrates the FinFET structure simulated in this study. The MC simulation results of temperature distribution were compared to those obtained by solving the heat conduction equation based on the Fourier's law, and significantly different hot spot temperature (ΔT ~ 95 K) was observed between the two methods. We then model the structure using equivalent thermal circuit. The magnitudes of thermal resistances were roughly estimated from the temperature difference across the heat path the heat flux. Finally, a rough estimation was made to assess the contribution of the gate electrode to remove the heat from the hot spot using additional heat path in the thermal circuit model. Fig. 2 shows the heat flux percentage through each heat path with the additional gate path to investigate its effect on the hot spot temperature.

Discussion: MC results exhibit larger thermal resistances compared to the Fourier law particularly in the paths from the Fin exit to the heat sink. This is due to the quasi-ballistic transport effect of phonons, which becomes significant when the system size is comparable or less than the phonon mean free path λ. Also, from the equivalent circuit and gate path addition, it has been found that the gate has a less significant, but non-negligible contribution, which would reduce the hot spot temperature slightly.

References: [1] C. Prasad et al., Proc. IRPS, p. 5D.1.1 (2013). [2] S. Lee et al., Tech. Dig. Symp. VLSI, p. T248 (2013). [3] K. Kukita et al., J. Appl. Phys. **114**, 154312 (2013). [4] I. N. Adisusilo et al., Proc. SISPAD (2014). .

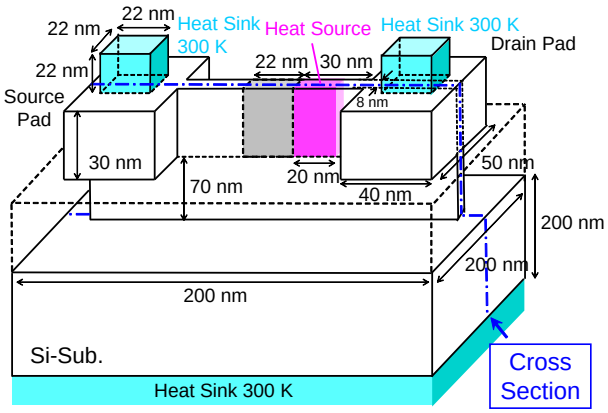

Fig. 1. Schematic view of the FinFET structure simulated in this study. The heat source was placed at the drain edge with a heat density of 7.1 TW/cm^3, and the constant-temperature reservoirs at 300 K were set on the top of the source/drain pads and below the bottom of the Si substrate.

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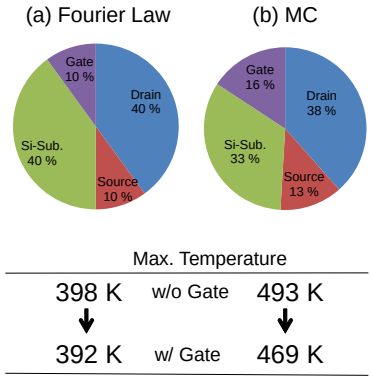

Fig. 2. (Top) Heat flow percentage through the gate electrode, Si substrate, drain, and source contacts, estimated from the equivalent circuit model based on the results of (a) Fourier law and (b) MC method. (Bottom) Change of the hot spot temperature before and after the insertion of the gate heat path.