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The Future of Micro and Nanoelectronics in the Zero Power and Zero Variability Era and the role of Cooperations

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The microelectronics industry is facing historical challenges to down scale CMOS devices through the demand for low voltage, low power, high performance and increased functionalities for nomadic applications. New progress laws combined to the scaling down of CMOS based technology will emerge to enable new paths to Functional Diversification. New materials and disruptive architectures, mixing logic, memories and sensors, Heterogeneous Integration 3D schemes at the Front and Back End levels, will come into play. International Cooperation will be a major engine for innovation.

1. Thin Films for Nanoelectronics scaling and the use of the 3rd dimension to continue Moore's law.

Fully Depleted CMOS devices using HiK /metal gate stacks and intentionally undoped Thin Films channels are key to flexible integration, continued scaling, and device electrostatics and drivability optimization[1]. Low Voltage, Low Power consumption circuits featuring good drivability and Low Variability can be designed thanks to Multigates wrapped around nanowires[1,2]. Tunneling Field Effect Transistors(TFET) with nanowires channels[2] reaching sub 60mV/dec will open the way to ultra low supply voltages(< 0.3V). With these architectures, nearly Zero Standby Power will be an opportunity but will request nearly Zero Variability[2]. The use of SOI substrates based platforms[3,4] eases the 3rd dimension heterogeneous integration by function partitioning and low temperature processing of new materials(HiK, Ge, III-V, 1D and 2D materials, …) without degrading their properties(Fig.1). The 3D co-integration of Logic and Memories[2], can increase bandwidth at low power consumption, introduce programmable, reconfigurable, neuromimetic architectures.

2. Interfacing the Multiphysics World by functional diversification and 3D at Wafer Level.

The connection of Nanoelectronics to the outside Multiphysics world requests diversified functionalities, i.e. selective sensing, actuation, imaging and displaying, power generation through available electrical, mechanical, ultra narrow band RF and High Frequency, photonic signals to address applications for societal needs. The Heterogeneous integration of new materials and devices within or with CMOS will require new 3D integration schemes[2]. Si based CMOS will be scaled beyond the ITRS as the System-on-Chip/Wafer Platform [2](Fig. 2). New systems based on hybrid associations could be co-integrated with or within CMOS [2] (Fig. 2). Complex challenges will require international cooperation between Fundamental Research, Integration Institutes and Industry including Education, in the frame of innovation campuses[6].

References

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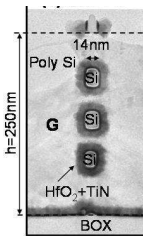
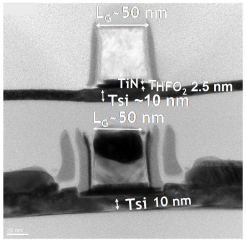


(a)



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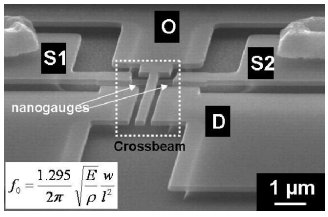
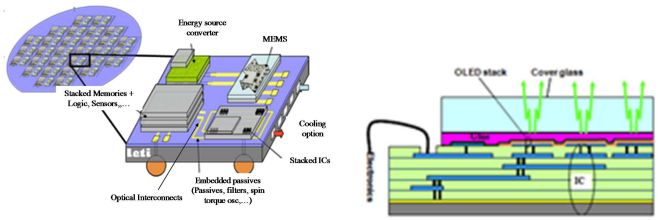


(c)

Figure 1 – Co integration in different ways:
a) Stacked nanowires ;
b)Sequential integration;
c) NEMS and CMOS



(a) (b)

Figure 2–Heterogeneous Hybrid co-Integration: a) 3D System on Wafer[2]; b) Near- eye OLED microDisplay on CMOS [5]

Figure 3 MINATEC Innovation Campus in Grenoble[6]