17p-PA2-9

III-V CMOS フォトニクス·プラットフォーム上 導波路型 InGaAs MSM フォトディテクタの作製

Fabrication of waveguide InGaAs MSM Photodetector on III-V CMOS Photonics Platform

東大院工 [1], 住友化学 [2]
○程勇鵬 [1], 一宮佑希 [1], 市川磨 [2], 長田剛規 [2], 秦雅彦 [2],竹中充 [1], 高木信一 [1]
Univ. Tokyo[1], Sumitomo Chemical Co. Ltd.[2]
○ Yongpeng Cheng[1], Yuki Ikku[1], Osamu Ichikawa[2], Takenori Osada[2], Masahiko Hata[2], Mitsuru Takenaka[1] and Shinichi Takagi[1]
E-mail: ypcheng@mosfet.t.u-tokyo.ac.jp

1. Background

For chip-scale optical interconnects, waveguide photodetectors (PDs) are fundamental building blocks; thus InGaAs PDs integrated with Si waveguides on the III-V/Si hybrid platform have intensely been investigated so far[1-3]. However, it seems to be difficult for the III-V/Si hybrid platform to achieve monolithic integration of InGaAs PDs with Si complementary metal-oxide-semiconductor (CMOS) transistors because high-temperature processes required for Si CMOS are not acceptable to InGaAs PDs. To overcome this constraint, we have investigated the III-V CMOS photonics platform[4,5], enabling monolithic integration of InGaAs MOS transistors and InP-based photonic devices on a III-V-on-Insulator (III-V-OI) wafer.

In this paper, we present a waveguide InGaAs metal-semiconductor-metal (MSM) PD on the III-V CMOS photonics platform.

2. Fabrication

Firstly, we prepare a III-V-OI wafer as follows. i-InP/p-InGaAs layers are grown on an InP wafer. A 2.3-μm-thick SiO_2 BOX layer is also thermally grown on a Si wafer. After depositing Al_2O_3 on both wafers by atomic layer deposition (ALD), the two wafers are bonded together. Finally, the InGaAs/InP on SiO_2/Si wafer is obtained by etching the InP substrate.

By using the III-V-OI wafer, we fabricate InGaAs MSM PD integrated monolithically integrated with an InP rib waveguide on the SiO_2/Si as shown Fig. 1. First, the waveguide is defined by DUV lithography and reactive ion etching (RIE). Then, an InGaAs layer on the InP waveguide is selectively removed by wet etching. Then, an Al_2O_3 passivation layer is deposited by ALD. Finally, interdigitated electrodes are formed by Ni deposition and lift-off.

3. Test and discussion

Firstly, 7.7dB total loss (insertion plus propagation loss) of the InP rib waveguide on the SiO_2/Si wafer is obtained by the cut-back method. Then, 8-dBm CW light is injected to compensate this loss and ensure approximately 0-dBm launched power to the InGaAs PD. We evaluate photo-current and dark current as shown by Fig. 2. Since Schottky contact can be obtained between Ni and p-InGaAs, the dark current is suppressed below approximately 270nA when the bias voltage is 1V. The photocurrent at 1V bias voltage is approximately 386μA when the 1550-nm CW light with the 0-dBm launched power to the PD is injected. Thus, the I_{on}/I_{off} ratio is approximately more than 10^3. When the bias voltage is increased to 2V, the photo-current of more than 1mA is obtained, resulting in the high responsivity of >1.0A/W.

Acknowledgements

This work was supported by Grant-in-Aid for Young Scientists (A) from MEXT.

Reference

[1] H. Park et al., OE 15, 6044 (2007).
[2] J. Brouckaert et al., PTL, 19, 1484 (2007).
[3] K. Ohira et al., OE 18, 15440 (2010).
[4] M. Takenaka et al., OE 15, 8422 (2007).
[5] M. Takenaka et al., OFC'10, OThS5 (2010).

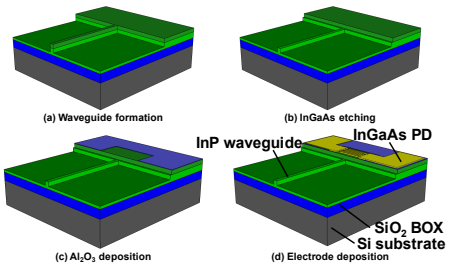

Fig. 1 Process flow InGaAs MSM PD.

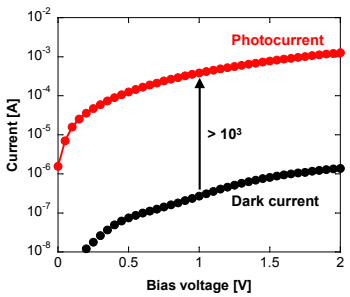

Fig. 2 Photo-current of InGaAs MSM PD.

© 2014 年　応用物理学会