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Effects of Annealing Ambient on the Electrical Properties of HfN Gate Insulator Formed by ECR Plasma Sputtering

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1. Introduction

Scaling down an equivalent oxide thickness (EOT) of high-κ gate insulator beyond 0.5 nm is a great challenge for next generation CMOS technology because of the formation of an interfacial layer (IL) between high-κ/Si interface. The IL with low dielectric constant increases the EOT [1]. We have reported that the 0.5 nm EOTs were obtained by using hafnium nitride (HfN) gate insulator formed by electron-cyclotron-resonance (ECR) plasma sputtering on both Si(100) and Si(110) substrates [2].

In this paper, the effect of annealing ambient dependence on the electrical characteristics of HfN gate insulator was studied. The effects of surface orientation including p-Si(100) and p-Si(110) were investigated for three-dimensional MOSFET device.

2. Experimental Procedure

First, p-Si(100) and p-Si(110) substrates were cleaned by SPM and DHF. Then HfN film (4 nm) was deposited by ECR plasma sputtering with the gas pressure of 0.20 Pa (Ar/N_2: 20/8 sccm) [3,4]. The deposited HfN films were annealed in the $Ar/4.9\%H_2$ and $N_2/4.9\%H_2$ forming gas (FG) ambient with the flow rate of 1 SLM at 500-600°C for 10-20 min. Finally, Al electrode (ϕ= 94 μm) was deposited by evaporation through a shadow mask. The C-V and J-V characteristics of Al/HfN/p-Si MIS diodes were measured. The density of interface states (D_{it}) was evaluated by Terman method.

3. Results and Discussion

Figures 1(a) and 1(b) show the C-V characteristics (100 kHz) of Al/HfN/p-Si(100) and Al/HfN/p-Si(110) MIS-diode, respectively. The $N_2/4.9\%H_2$ FG annealing has better capability for hydrogen passivation at the HfN/Si interface and/or in the HfN film on both Si(100) and Si(110) surface compared to $Ar/4.9\%H_2$ FG annealing. By using $N_2/4.9\%H_2$ FG annealing at 500°C/20 min, similar C-V characteristics with an EOTs of 0.47 and 0.51 nm with leakage current density, J_g, ($@V_{FB}$ -1 V) of 1.1 and 1.4 A/cm^2 were obtained on Si(100) and Si(110) substrates, respectively. By annealing the samples in $Ar/4.9\%H_2$ FG ambient at 600°C/10 min, EOTs of 1.0 and 0.82 nm with low J_g ($@V_{FB}$ -1 V) of 3.9×10^{-5} and 6.4×10^{-5} A/cm^2 were obtained on Si(100) and Si(110) substrates, respectively. The D_{it} with the order of 10^{11} cm^{-2}eV^{-1} was obtained on both substrates after annealed in both FG ambients.

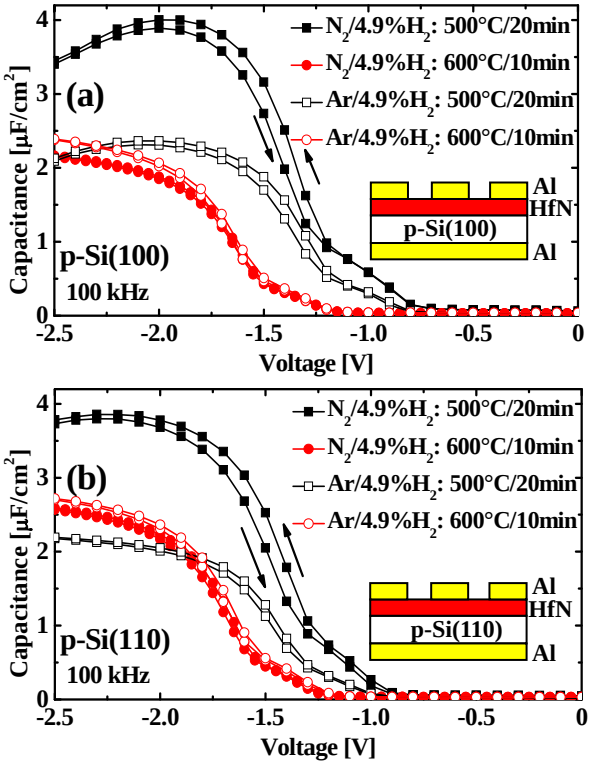

Fig. 1. C-V characteristics of Al/HfN/p-Si (100 kHz) annealed in $Ar/4.9\%H_2$ and $N_2/4.9\%H_2$ FG ambient at 500°C/20 min and 600°C/10 min. (a) Si(100) and (b) Si(110).

4. Conclusions

We investigated an effect of annealing ambient dependence on the diode characteristic of HfN gate insulator formed by ECR plasma sputtering. The EOTs below 0.5 nm were obtained on both Si(100) and Si(110) substrates by $N_2/4.9\%H_2$ FG annealing at 500°C/20 min.

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References

[1] Y. Morita, *et. al.*, Appl. Phys. Lett., **2** (2009) 011201-1.

[2] N. Atthi, *et. al.*, The 74th JSAP autumn meeting (2013) 17p-B5-9.

[3] H.-S. Han and S. Ohmi, IEICE Electron. Express, **9** (2012) 1329.

[4] N. Atthi, *et. al.*, JSAP-MRS joint symposia, (2013) 18p-PM1-32.