Effects of biaxially-tensile strain on properties of Si/SiO₂ interface states generated by electrical stress [°]W.-L. Cai^{1,2}, M. Takenaka^{1,2} and S. Takagi^{1,2}

School of Engineering, The University of Tokyo¹, 2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-8656, Japan, JST CREST²

caiweili@mosfet.t.u-tokyo.ac.jp

INTRODUCTION Strained-Si (sSi) MOS devices have widely been used for advanced CMOS devices, because of the high carrier mobility [1]. On the other hand, any reliability issues of sSi MOS devices and, in particular, the impact of the channel strain on the degradation of SiO₂/sSi MOS interfaces under electrical stress are critical issues for making full advantages of sSi MOS devices. Actually, there have been several experimental results on the reliability issues of SiO₂/sSi interfaces [2]-[4]. It has been reported that ΔV_{th} of MOSFETs after FN stress becomes smaller with increasing tensile strain [2]. However, to our best knowledge, systematic characterizations of SiO₂/sSi interface states and the generation by electrical stress as a function of channel strain in channels have not been performed yet.

In this paper, the properties of interface states at SiO₂/sSi interfaces, generated by Folwer-Nordheim (FN) stress, have been examined in the terms of the density of interface state (D_{it}) as a function of strain. On the other hand, ΔV_{th} of SiO₂/sSi MOSFETs after the stress is also examined. It is found, as a result, that ΔV_{th} is dependent on the strain, while *Dit* is almost independent of the strain. An E_{CNI} -based interface state charging model has been proposed to explain this different strain dependence.

EXPERIMENTAL The bi-axial tensile strain Si nMOSFETs on relaxed p-SiGe buffers were used. The structure of n-MOSFETs used in this experiment is shown in Fig. 1. Biaxially tensile strained Si layers were epitaxially grown on relaxed SiGe. The amount of tensile strain was modulated by the Ge contents ranging from 10 to 30 %. The gate area of MOSFETs was 100 µm x 100 μ m. Interface states were introduced by positive FN injection from the substrate with constant current density (1x10⁻³ A/cm²). The energy distribution of D_{it} in the valence band and conduction band sides was analyzed by the conductance method [5] and the subthreshold slopes of MOSFETs [6], respectively.

RESULTS AND DISCUSSION Firstly, the results on n-MOSFETs before and after FN stress are shown. Fig. 2 shows ΔV_{th} extracted from C-V curves of MOSFETs after FN stress. It is

observed that ΔV_{th} tends to decrease with increasing tensile strain, which is consistent with the results in [2]. On the other hand, D_{it} in the valence band side, determined by the modified conductance method [9] (Fig. 3), has almost no strain dependence or slightly increases with increasing strain. This result does not simply match with the result of ΔV_{th} . It should be noted, however, that ΔV_{th} of n-MOSFETs is related more directly to D_{it} in the conduction band side, which needs to be accurately evaluated. In order to evaluate the energy distribution of D_{it} in the conduction band side for n-MOSFETs, the S-factor method was employed in this study. The obtained energy distributions of D_{it} in the conduction band side are shown in Fig.4. It is found that D_{it} in the conduction band side also slightly increases with increasing strain, which cannot explain the ΔV_{th} result shown in Fig. 2, neither. In order to quantitatively examine ΔV_{th} , the charge neutrality level (E_{CNL}) based model (Fig.5) has been proposed. This model assumes that E_{CNL} does not change its energy position with respect to the vacuum energy level (E_{vac}) . Fig. 6 shows the experimental and calculated ΔV_{th} . Although there is no perfect match, the considerations on E_{CNL} can provide better representation of the strain dependence of ΔV_{th} after FN stress.

CONCLUSION The larger D_{it} and smaller ΔV_{th} in sSi n-MOSFETs after FN stress can be reconciled by the relative shift of E_{CNL} inside the band gap of strained Si.

ACKNOWLEDGMENT This work has been supported by Semiconductor Technology Academic Research Center (STARC). We would be grateful to Dr. M. Saitoh in Toshiba Corporation and Dr. T. Yamashita in Renesas Electronics.

References [1] S. Takagi et al., JAP, 80, 1567(1996). [2] Y. Zhao et al., TED, 32, 1005(2011). [3] J. R. Shih et al., 43rd IRPS, 403 (2005). [4] T. Irisawa et al., TED, 55, 3159(2008). [5] E. H. Nicollian et al., MOS Physics and Technology (Wiley, New York, 1982), Chap. 5. [6] S. M. Sze et al., Physics of semiconductor devices, Chap.6. [7] N. Shiono et al., APL, 48, 1129(1986). [8] S. Takagi et al., TED, 45, 494(1998). [9] W. Cai et al., Silicon Nanoelectronics Workshop, 25(2013).



Fig. 4. D_{it} energy distribution in conduction band side determined by S-factor method.



Fig. 2. The threshold voltage shift of C-V curves after FN stress.



Fig.5. Energy band diagrams of E_{CNL}-based model.



Fig.3. D_{it} energy distribution in valence band side determined by conductance method.



Fig.6. Comparison of ΔV_{th} between calculation result and experiment one