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低界面準位と sub-nm CET を有する $La_2O_3/In_{0.53}Ga_{0.47}As$ ゲートスタックの実現

Low D_{it} $La_2O_3/In_{0.53}Ga_{0.47}As$ Gate Stack scaled to sub-nm CET

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【Introduction】Integration of high-mobility channels such as InGaAs is envisaged for beyond 10-nm node devices [1]. However, fabrication of high quality high-k/III-V interface with low interface trap density remains a key issue. Overwhelming majority of InGaAs device demonstrations use Al_2O_3 as gate dielectric, which benefits from good interface properties. Consequently scaling of InGaAs-based gate stacks has been limited due to low k-value (~9) of Al_2O_3. However, high C_{ox} values in quasi-ballistic regime of 10-nm node and beyond is required to minimize the effect of high semiconductor capacitance and improve gate controllability [2]. In this study, we have demonstrated a scalable La_2O_3/InGaAs gate stack with La_2O_3 deposited either by EB or ALD methods with equal interface quality, thanks to the formation of an amorphous interfacial layer at the La_2O_3/InGaAs interface.

【Experiments】La_2O_3-gated devices were fabricated on *n*-$In_{0.53}Ga_{0.47}As$ substrates (dopant: 1.0×10^{16} cm^{-3}). Substrates were first, treated by HF and $(NH_4)_2S$ (6%) solution prior to La_2O_3 deposition. ALD-La_2O_3 films were grown from precursors lanthanum tris(isopropylcyclopentadienyl) and H_2O at various deposition temperatures. Bi-layer TiN/W metal gates were in-situ deposited by RF sputtering. A gate last scheme was used to fabricate InGaAs MOSFETs on *p*-$In_{0.53}Ga_{0.47}As$ (dopant: 1.8×10^{17} cm^{-3}) with a similar gate stack process flow to capacitors.

【Results】Conductance measurements were carried out to evaluate the interface trap density (D_{it}) at La_2O_3/InGaAs interface. The results compared to other recently reported high-k materials is shown in Fig. 1 (a). Small D_{it} on the order of 10^{11} (cm^{-2} eV^{-1}) is achieved for La_2O_3/InGaAs capacitors even at sub-nm CET values. The similarity of results between deposition methods can be attributed to the presence of interfacial layer in the form of $LaInGaO_x$ which is formed reactively at InGaAs interface. InGaAs MOSFET operation with ALD-La_2O_3 as gate dielectric and Ni as metal S/D is demonstrated in Fig. 1(b). Mobility exceeding that of Si-universal is achieved for a gate stack with CET= 1.1 nm.

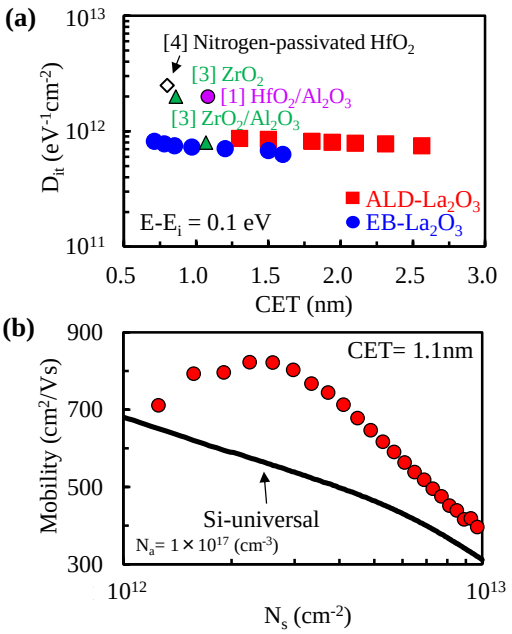

Fig.1 (a) D_{it} dependence on CET for La_2O_3/InGaAs and (b) effective electron mobility of nMOSFETs measured by split C-V.

【References】

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