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容量―電圧特性から推定した high-k/InGaAs MOS キャパシタの酸化膜トラップ分布

Determination of oxide traps distribution in high-k/InGaAs MOS capacitor by capacitance-voltage measurement

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Introduction: To realize high performance III-V based n-MOSFETs, a crucial issue arousing increasing attention is the existence of large amounts of oxide traps near or above the conduction band minima, which may degrade on-state performance of the devices severely [1]. In this study, we propose a method to determine the distribution of oxide traps in energy and space by an empirical model to evaluate the frequency (*f*) and temperature (*T*) dependent response of oxide traps using the equations summarized in Table I.

Model description: The time constant of oxide traps, τ_{bt}, can be given by Eq. 1 [2], where τ_0 is the time constant at the interface, κ is the tunneling decay factor and x is the distance from the interface into the oxide. τ_0 can be given by Eq. 2, where N_C is density of conduction band states, σ is the capture cross-section and v_{th} is the thermal velocity. The temperature dependency of τ_0 is inferred to be dominated by thermal activated σ governed by Eq. 3 [3], where σ_0 is the pre-factor and E_b is the activation energy. Therefore, the temperature and frequency dependent probing depth, X_P, can be given by Eq. 4. Adopting commonly used parameters for $In_{0.53}Ga_{0.47}As$, the X_P at 100 Hz and 1 MHz as a function of temperature is shown in Fig. 1.

Results and discussion: X_P decreases with increasing frequency or decreasing temperature. In the 100 Hz to 1 MHz C-V measurement (Fig. 1), while the response of the oxide traps reside in Region I/III is too fast/slow to be detected, the oxide traps in Region II contribute to the frequency dispersion of the C-V curves in accumulation. Therefore, the temperature dependent frequency dispersion in accumulation actually reflects the spatial distribution of oxide traps. A method to profile the oxide traps is proposed and the result is shown in Fig. 2. .

Reference: [1] M. Heyns, et al., *IEDM*, pp. 299-302 (2011). [2] F. P. Heiman, et al, *IEEE Trans. Electron Devices*, vol. ED-12, no. 4 (1965). [3] D. K. Schroder, Semiconductor Material and Device Characterization, New York : Wiley (2006).

Table I. Summary of the equations used to evaluate the probing depth:

Time constant of border traps:

$$\tau_{bt} = \tau_0 e^{2\kappa(E)x} \quad \text{Eq. (1)}$$

$$\tau_0 \approx (N_C \sigma v_{th})^{-1} \quad \text{Eq. (2)}$$

Temperature dependency of σ:

$$\sigma = \sigma_0 \exp\left(-\frac{E_b}{kT}\right) \quad \text{Eq. (3)}$$

Evaluation of probing depth:

$$X_P = \frac{1}{2\kappa} \ln \frac{1}{2\pi f \tau_0} \quad \text{Eq. (4)}$$

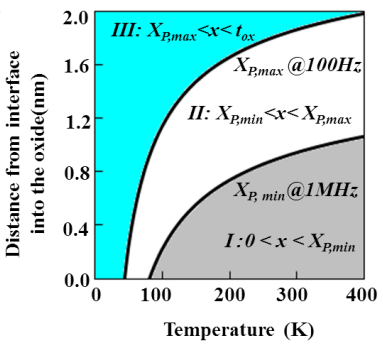

Fig. 1. Probing depth at 100 Hz and 1 MHz as a function of temperature

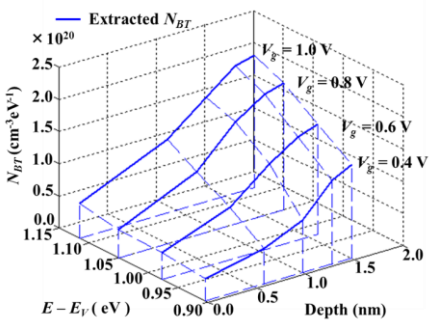

Fig. 2. Extracted oxide traps distribution in energy and space in high-k/InGaAs MOSCAP