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Type-II Staggered Hetero-Junction Tunnel FETs with Ge sources and Biaxial Tensile Strain Si Channels

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1. Introduction While tunnel field-effect transistors (TFETs) based on band-to-band tunneling are expected as ultra-low power devices, it is still difficult to experimentally achieve both high drain on-current/off- current ratio (I_{on}/I_{off}) and low subthreshold swing of sub-60 mV/dec at the same time. Here, a type-II staggered hetero-structure source junction can enhance I_{on} of nTFETs without increasing the leakage current. Actually, a Si-channel TFET with a Ge-source has been demonstrated [1]. Furthermore, the introducing of a tensile strain into a Si channel boosts the tunneling possibility due to increased electron affinity and decreased energy band-gap (E_g) of Si [2]. In this paper, Ge/sSi hetero-junction TFETs have been experimentally demonstrated by using growing Ge thin films on strained-SOI substrates.

2. Experiment The fabricated device structure and the band diagrams near the Ge-source/sSi-channel are schematically illustrated in Fig. 1(a) and (b), respectively. Dashed lines indicate the band diagrams of unstrained Si. The small E_g of Ge as the source and s-Si with biaxial tensile strain as the channel lead to the type-II staggered hetero-structure. Fig. 2 shows the process flow of the proposed device. Commercial strained silicon-on-insulator (sSOI; 1.1 % tensile stain) substrates are used for starting materials. Phosphorus ion implantation is used for drain formation with low acceleration energy of 10 keV, followed by RTA at 900 °C for activation. 25-nm-thick in situ boron-doped Ge layers are grown at 200 °C on the drain-formed substrates by molecular beam epitaxy. 2-step 3-nm-thick Al_2O_3 deposition is done by atomic layer deposition with electron cyclotron resonance plasma post oxidation to ensure the high quality MOS interface between Al_2O_3 and Ge [3]. Ta is deposited as the gate metal, followed by Ni and Al deposition for the source contact and the contact pad, respectively. Forming gas annealing is carried out at 400 °C in 4% H_2/N_2 mixed gas ambient for 30 minutes.

3. Results and Discussion Fig. 3(a) and (b) show the drain current-gate voltage (I_d-V_g) and the drain current -drain voltage (I_d-V_d) characteristics, respectively, of a fabricated device. The small minimum subthreshold swing of 51 mV/dec, below the thermal limit, is obtained (inset of Fig. 3(a)) with large I_{on}/I_{off} over 6 orders of the magnitude. Also, the good saturation current is confirmed in Fig. 3(b).

3. Conclusions The hetero-junction TFET fabricated by combining in-situ boron doped epitaxial-Ge on strained-SOI substrates with Al_2O_3-based Ge gate stacks are demonstrated.

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References [1] S. Kim et al., Symp. VLSI Tech. Digest (2009) 178. [2] Q. T. Zhao et al., IEEE Electron Device Lett., 32 (2011) 1480. [3] R. Zhang et al., Appl. Phys. Lett., 98, (2011) 112902.

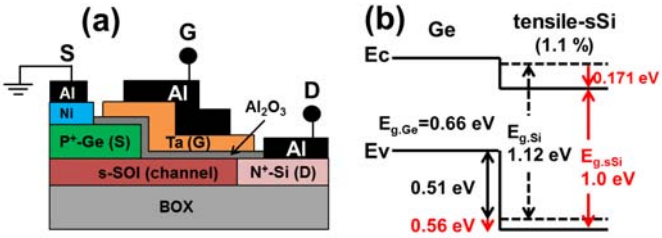

Fig. 1(a) Device structure and (b) band diagrams of Ge-source/sSi-channel hetero-junction.

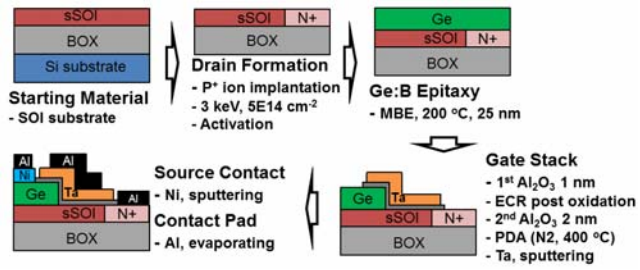

Fig. 2 Process flow of the proposed device.

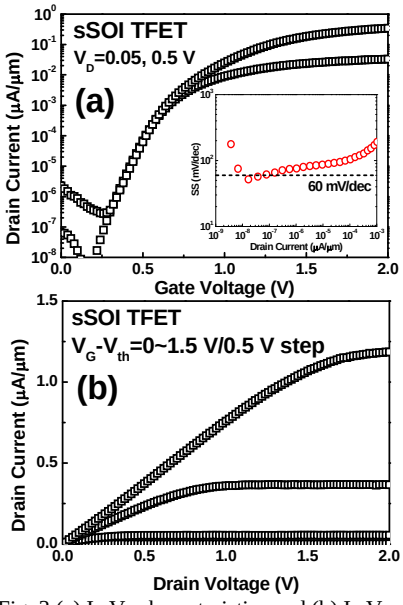

Fig. 3 (a) I_d-V_g characteristics and (b) I_d-V_d characteristics of the proposed device.