Variation Behaviors of Tunnel-FETs and MOSFETs Compared on an SOI

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Tunnel-FETs (TFETs) control the band-to-band tunneling (BTBT) current flow by the gate bias [1]. This operation mechanism has a potential to reduce the subthreshold swing (SS) to be less than 60 mV/decade, which is the theoretical limit of conventional MOSFETs at room temperature. TFETs are expected to reduce the operation voltage of FETs, and contribute to the development of ultra low-power VLSIs. Variation of electrical characteristics among many devices is a critical issue for VLSI, and has been actively studied in MOSFETs [2]. It is a common issue for TFETs, and a simulation study reported that variation of TFETs would be different from that of MOSFETs [3]. In this work, we experimentally compared the variation behavior of TFETs and MOSFETs fabricated on an SOI substrate, and studied the origins of their difference using simulation.

P-type TFETs and n-type MOSFETs were fabricated on an SOI substrate using a conventional gate-first process (Fig. 1). The gate stack structures, ion implantation and annealing conditions are the same. The drain region of TFETs is offset from the gate edge by a tilted angle implantation in order to suppress the ambipolar current flow. Electrical characteristics of 50 devices of p-TFETs and n-MOSFETs with 500 nm gate length and 1 μm width are shown in Fig. 2. Co-production of TFETs and MOSFETs on an SOI substrate is successfully demonstrated. Because of the limitations of material (Si has an indirect band) and process (EOT scaling and abruptness of junction), the SS of TFETs in this work is remained to be around 140 mV/decade. The variations of $I_D/I_{D0}$ at respective gate bias conditions are plotted in Fig. 2. Both TFETs and MOSFETs show a similar trend that the variation is large for subthreshold region and becomes small at strong gate bias conditions. However, it is of interest that absolute value of variation for TFETs is always larger than those for MOSFETs in whole gate bias region. Variation will be more serious in TFETs as far as they are prepared by the same process technique with MOSFETs.

The origin of larger variation in TFETs is studied by simulation using non-local BTBT model [4]. Sensitivity of drain currents with gate stack parameters, equivalent oxide thickness (EOT) and work function of metal gate (WF), are summarized in Fig. 3. The trends of experimental results are reproduced in simulation. At subthreshold regions, the variations are caused by the fluctuation of WF, and at strong gate bias conditions, the variation are dominated by the fluctuation of EOT. It is observable that the variation becomes larger for TFETs when the fluctuations of gate stack parameters are the same with MOSFETs. In order to confront with the variation of TFETs, therefore, a strict control of device parameters such as EOT and WF is indispensable.

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