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Record-high Electron Mobility in Sub-nm EOT Ge n-MOSFETs with Y-doped GeO_2 Interfacial Layer

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[Introduction] We have examined the effect of metal cation (Y, Sc, Al, Hf) doping into GeO_2 on improvements of thermal stability and water solubility as well as interface properties [1-3], and trivalent metal cation (Y and Sc) seemed to be the most effective way to overcome the intrinsic disadvantages of pure GeO_2 interfacial layer (IL). The objective of this work is to verify our IL engineering for sub-nm EOT Ge MOSFETs. The EOT scaling of high-*k* gate stacks on Ge with Y-doped GeO_2 (YGO) IL is first provided, and the record-high electron mobility in 0.7 nm EOT Ge n-MOSFETs is demonstrated for a wide range of N_s.

[Experiment] To achieve sub-nm EOT gate stacks with superior interface properties, YGO formation on Ge was optimized. 1 nm-thick YGO was deposited on Ge by co-sputtering of Y_2O_3 and GeO_2 targets. The thickness and chemical states of YGO were estimated by Ge 3*d* core level spectra of XPS measurements, and the atomic concentration of Y was estimated by Y/Ge atomic composition ratio in YGO. Then, HfO_2 was deposited on 1 nm-thick 10% YGO IL to examine the EOT scaling with YGO IL. PDA was carried out at 500°C for 30 sec in N_2/O_2 (0.1%) ambient. Finally, Ge n-MOSFETs were fabricated on atomically flat Ge(111) surface [4] to verify our IL engineering concept.

[Results and Discussion] **Fig. 1** shows bidirectional *C-V* curves of Au/HfO_2/YGO/Ge stacks measured at 1 MHz. A very small hysteresis (~20 mV) and no V_{FB} shift indicate the excellent interface properties similar to YGO/Ge stacks. Note that HfO_2/YGO/Ge stack is thermally stable up to 550°C without interface degradation. 0.47 nm-thick EOT on Ge was achieved with 1 nm-thick HfO_2/YGO(1 nm)/Ge stack, which is one of the lowest EOT on Ge gate stacks. Excellent gate leakage current and superior interface properties of HfO_2/YGO/Ge stack are originated from strong barrier properties of YGO against oxygen. This is clear evidence that our thermodynamic-based guideline for YGO IL on Ge is valid for gate stack formation. The high-N_s electron mobility benchmark in the sub-nm region of Ge n-MOSFETs is shown in **Fig. 2**, which indicates that the present results are far above the results reported so far. Both the highest peak mobility (828 cm^2/Vs) and high-N_s mobility (437 cm^2/Vs) in Ge n-MOSFETs with 0.7 nm EOT were demonstrated, which is two times higher than the scaled Si n-MOSFETs. Note that the enhancement of high-N_s electron mobility in HfO_2/YGO/Ge stack was observed by maintaining atomically flat YGO/Ge interface similar to GeO_2/Ge one [5]. This can be achieved by superior bulk and interface properties of YGO IL, and further EOT scaling is possible without a cost of mobility degradation thanks to thermodynamically robust YGO IL.

[Reference] [1] C. H Lee *et al.*, *VLSI* (2013). [2] C. Lu *et al.*, *IWDTF*, 5 (2013). [3] C. Lu *et al.*, *JSAP* spring MTG (2014). [4] T. Nishimura *et al.*, *APEX*, **5**, 121301 (2012). [5] C. H. Lee *et al.*, *JSAP* spring MTG (2014).

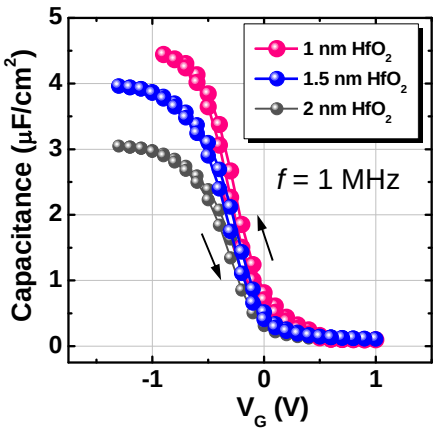

Fig. 1 Bidirectional *C-V* characteristics of HfO_2/YGO/Ge stacks. It shows good *C-V* curves similar to YGO/Ge stack, and 0.47 nm-thick EOT on Ge was achieved with 1 nm-thick HfO_2/YGO(1 nm)/Ge stack.

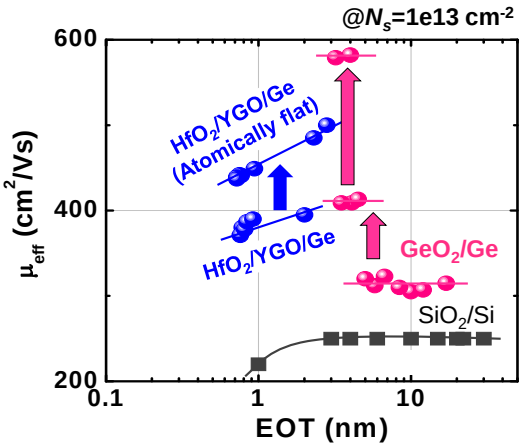

Fig. 2 High-N_s electron mobility as a function of EOT at N_s =1x10^{13} cm^{-2}. The highest high-N_s mobility of 437 cm^2/Vs in Ge n-MOSFETs with 0.7 nm EOT is demonstrated. This can be achieved by superior interface properties of YGO IL.