[Vth] Shifts and Their Variability Behaviors in pFETs by High Voltage ON-State and OFF-State Stress
Nurul Ezaila Alias, Anil Kumar, Takuya Saraya, and Toshiro Hiramoto
Institute of Industrial Science, University of Tokyo
E-mail: alias@nano.iis.u-tokyo.ac.jp

[Introduction] Recently, a new concept of a post-fabrication self-improvement technique of SRAM cell stability by simply applying high voltage to VDD terminal has been proposed and demonstrated [1-3]. In this technique, ON-state stress is selectively applied to a stronger pFET in each cell and [Vth] increases, while OFF-state stress is selectively applied to a weaker pFET and [Vth] decreases, resulting in automatic cell stability improvement [3]. It has been found that pFET reliability after high voltage stress is not a problem [4] and has no critical recovery issue [5]. In this study, systematic measurements of [Vth] and their variability in pFETs by ON-state and OFF-state stress is performed. It is found that [Vth] in pFETs by high voltage ON-state and OFF-state stress depends on gate length (L) and gate width (W). It is also found that variability of [Vth] by ON-state stress shows normal distribution and roughly follows the Pelgrom plot, indicating that the total trapped charges by ON-state stress are randomly placed.

[Method] Device matrix array (DMA) TEG of pFETs with various L and W was fabricated by the 65nm bulk technology. The ON-state and OFF-state stress were applied at 100°C for 10 sec. [Vth] of each transistor before and after stress was measured. Then [Vth] was calculated and [Vth] were derived. Please note that both OFF-state and ON-state stress has higher stress voltage and very short stress time.

[Results] Fig. 1 (a) shows measured mean [Vth] of pFETs by ON-state stress as a function of W for various L. Strong dependences on both W and L were observed, and the largest [Vth] was observed in the smallest pFET (L=60nm, W=120nm). This strange width dependence behavior may be due to the effect of shallow trench isolation (STI) [6]. Fig. 1 (b) shows measured mean [Vth] of pFETs by OFF-state stress as a function of W. It is found that pFETs by OFF-state stress shows two different phenomena: negative [Vth] (the device is strengthened) in narrower pFETs and positive [Vth] (weakened) in wider pFETs. Fig. 2 (a) shows cumulative plot of [Vth] by ON-state stress is caused by a statistically random process. Therefore, a simple model of sigma [Vth] is derived and compared with the measurement data as shown Fig. 2 (b). The saturation behavior of sigma [Vth] is well reproduced and supports the model where the total trapped charges after the ON-state stress are randomly placed and follows the random process.

[Conclusion] [Vth] shifts in pFETs by high voltage ON-state and OFF-state stress has strong transistor size dependence. The variability of [Vth] shifts by the ON-state stress roughly follows both normal distribution and Pelgrom plot, indicating that the [Vth] shifts is caused by random charge trapping process.