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High Mobility Ge CMOS Devices with Ultrathin EOT Gate Stacks Fabricated by Plasma Post Oxidation

Rui Zhang, Mitsuru Takenaka and Shinichi Takagi
School of Engineering, The University of Tokyo
E-mail: zhang@mosfet.t.u-tokyo.ac.jp

Introduction It has been increasingly difficult to further improve the performance of Si MOSFETs by conventional device scaling down [1]. Therefore, the employment of high mobility channel materials has been considered as one of the most promising solutions to enhance the CMOS devices performance [2]. Ge has been attracting a lot of interest as the channel material for MOSFETs, due to its much higher mobility for both hole and electron compared with those in Si [3-5].

Although high mobility Ge MOSFETs has been realized by using the thick GeO_2/Ge gate stacks [6-8], EOT scaling using high-*k* dielectrics is mandatory to realize high performance Ge MOSFETs. However, it has been found that the mobility is severely decreased in thin EOT high-*k*/Ge MOSFETs, attributable to the degradation of Ge MOS interface qualities. Thus, the formation of advanced Ge gate stacks with both ultrathin EOT and good interface qualities (low D_{it}) is the critical issue to obtain superior Ge MOSFETs. In this research, we demonstrate a plasma post oxidation (PPO) technique to oxidize the Ge surface by using oxygen plasma exposure to ALD high-*k*/Ge structures. Here the high-*k* layer serves as the oxygen barrier to prevent the growth of unnecessarily thick GeO_x interfacial layer (IL), as well as the protection layer to eliminate any damage to the ultrathin GeO_x/Ge interface after its formation. As a result, the high-*k*/GeO_x/Ge gate stacks have been formed with sub-nm EOT and low D_{it} simultaneously. The high mobility Ge MOSFETs have also been realized by using these gate stack structures.

Formation of high-*k*/GeO_x/Ge gate stacks Fig. 1 shows the fabrication procedure of Ge gate stacks with PPO method. The HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/Ge structures were formed by ALD deposition. After that, the samples were exposed to electron cyclotron resonance (ECR) oxygen plasma. The formation of the GeO_x IL is confirmed by using XPS after the PPO of HfO_2/Al_2O_3/Ge structures with a 500 W plasma for 15 s at room temperature, without inter-mixing between the GeO_x and high-*k* layers (data not shown). It is confirmed from the cross section TEM image that the GeO_x IL exhibits a thickness of 0.35 nm and a clear interface with the Ge surface. The Au/HfO_2/Al_2O_3/GeO_x/Ge MOS capacitors were fabricated with this gate stack structure and an EOT of 0.76 nm and D_{it} of 2×10^{11} $cm^{-2}eV^{-1}$ have been obtained.

High mobility Ge CMOS devices The Ge p- and n-MOSFETs were fabricated using a gate-first process using these HfO_2/Al_2O_3/GeO_x/Ge gate stacks. The normal operations of these devices has been confirmed from the I_d-V_g characteristics shown in Fig. 3. The S factors of 85 and 80 mV/dec have been realized for the Ge p- and n-MOSFETs, respectively, indicating the sufficient passivation of Ge MOS interfaces by using the PPO HfO_2/Al_2O_3/GeO_x/Ge gate stack. The mobility in these Ge p- and n-MOSFETs were evaluated using split C-V method. It is found that high peak mobility of 546 and 689 cm^2/Vs is achieved with an EOT of 0.76 nm, attributable to the sufficient reduction of D_{it} at the Ge MOS interfaces (Fig. 4).

Conclusion We have demonstrated a plasma post oxidation method yielding superior high-*k*/GeO_x/Ge gate stacks with ultrathin EOT in sub-nm range and low D_{it} at 10^{11} $cm^{-2}eV^{-1}$ level. High mobility Ge p- and n-MOSFETs have been realized with ultrathin EOT of ~0.7 nm. There results indicate the feasibility of the PPO method in future high performance MOSFETs technology with Ge channels.

References [1] E. J. Nowak. *IBM J. Res. Rev.*, pp. 169, 2002. [2] S. Takagi, et al. *IEDM*, pp. 57, 2003. [3] K. C. Saraswat, et al, *Microelectron. Eng.*, pp. 15, 80, (2005). [4] S. Takagi, et al., *Microelectron. Eng.*, pp. 2314, 84 (2007). [5] A. Toriumi, et al., *Microelectron. Eng.*, pp. 1571, 86 (2009). [6] Y. Nakakita et al., *IEDM*, pp. 877, 2008. [7] K. Morii, et al. *IEDM*, pp. 681, 2009. [8] C. H. Lee, et al. IEDM, pp. 416, 2010.

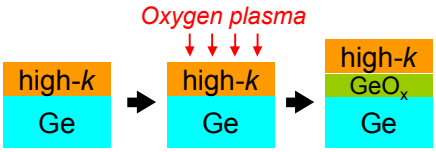

Fig. 1. The fabrication process of high-*k*/GeO_x/Ge gate stacks by plasma post oxidation.

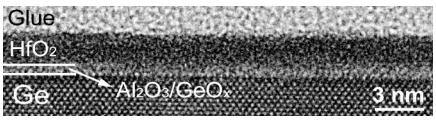

Fig. 2. The cross section TEM image of an ALD HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/Ge structure after PPO.

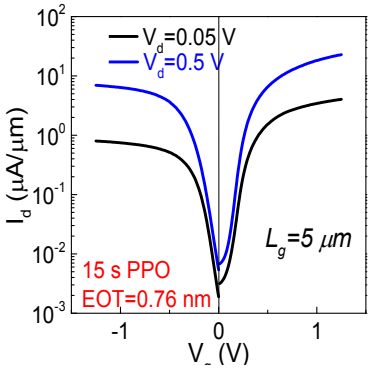

Fig. 3. The I_d-V_d characteristics of Ge p- and n-MOSFETs with HfO_2/Al_2O_3/GeO_x/Ge gate stacks.

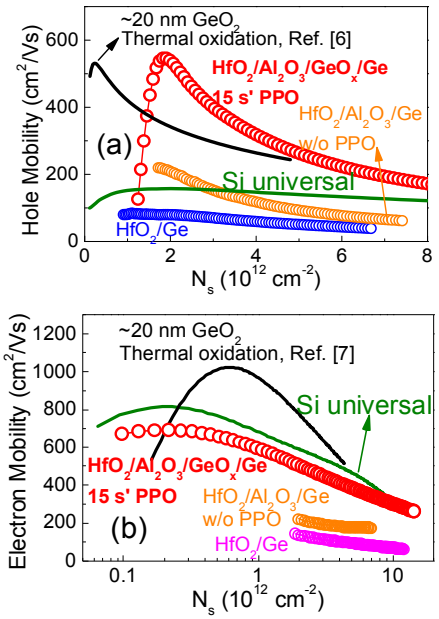

Fig. 4. The hole (a) and electron (b) mobility of Ge p- and n-MOSFETs with $HfO_2Al_2O_3$/GeO_x/Ge gate stacks.