Impact of back interface passivation on electrical properties of ultrathin-body Germanium-on-insulator (GeOI) MOSFETs

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Introduction Ge CMOS has been regarded as a promising device for the future logic LSIs. Here, ultrathin-body (UTB) Ge-on-insulator (GeOI) structures [1-3] are strongly needed to enhance the immunity against short channel effects, which is mandatory for scaled MOSFETs. It has been reported [4] that the commercial Smart-CutTM GeOI has the problems of the poor crystalline quality of GeOI near the Ge/ buried oxide (BOX) of SiO_2 as well as the poor Ge/SiO_2 interfacial quality. In order to solve these problems, we have proposed and demonstrated a novel way to fabricate GeOI substrates through layer transfer technology utilizing the high quality surface layers of Smart-Cut GeOI as well as back interface passivation [5]. However, the influences of the back interface passivation and the crystallite quality on the device characteristics have not been discriminate yet.

In this study, UTB GeOI MOSFETs with different Ge/BOX back interfaces are fabricated and the electrical properties are evaluated. The GeOI thickness dependence of the interfacial quality and the effective hole mobility are systematically examined among different GeOI structures.

Experimental Three different GeOI substrates with the different Ge/BOX back interfaces were prepared as follows. Besides the original Smart-Cut GeOI, the flipped GeOI with or without back interface passivation were utilized. The process flow of the flipped GeOI fabrication is shown in Fig.1. Here, the Al_2O_3/GeO_x/Ge back interface, formed by electron cyclotron resonance (ECR) plasma post oxidation (PPO) after the Al_2O_3 deposition [6], and the Al_2O_3/Ge back interface without PPO were fabricated before bonding, as shown in Fig. 1(b) and (c).After the GeOI substrate fabrication, back gate MOSFETs with metal source/drain were fabricated with the different GeOI thickness.

The average value of the interface trap density (D_{it}) estimated from the sub-threshold slope (S.S) of I_d-V_g curves and the effective hole mobility of 20 nm GeOI with the different back interfaces are shown in Fig. 2 and Fig. 3, respectively. It is found that the trend of the mobility is consistent with that of the estimated D_{it} value, indicating the back interfacial quality is more critical to the mobility than the crystallite quality at a given thickness.

The thickness dependence of average D_{it} estimated from the S.S factors of the different GeOI back interface are shown in Fig. 4. It is observed that the Dit values are almost constant with reducing the GeOI thickness, indicating the back interfacial quality is maintained even in the UTB region. Fig. 5 shows the GeOI thickness dependence of the hole mobility in comparison with the reported data [4]. It is shown that, when the GeOI thickness reduces to around 10 nm in the UTB region, the mobility among GeOI with the different interfaces tends to merge. These results mean that, in the UTB region, any other scattering mechanisms than the back interfacial quality would dominate the mobility.

Conclusion The electrical properties as well as the thickness dependence of UTB GeOI MOSFETs with the different back interfaces have been evaluated. The interfacial quality has been found to be critical to the GeOI effective mobility than the crystallite quality.

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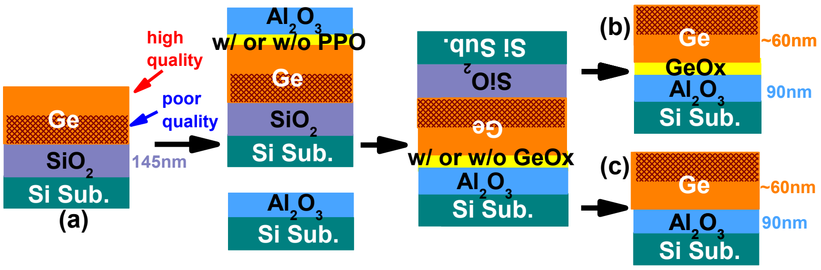

Fig.1: Process flow of flipped GeOI fabrication and the GeOI with different back interface(a) original GeOI (b) flipped GeOI with PPO (c)flipped GeOI w/o PPO

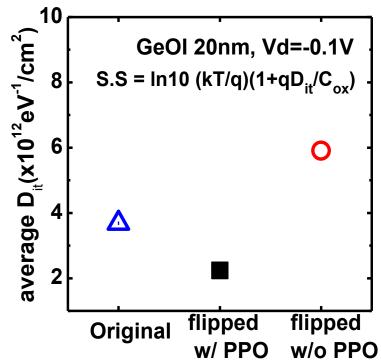

Fig.2: Average value of D_{it} estimated from the S.S factors of 20nm GeOI with different back interface

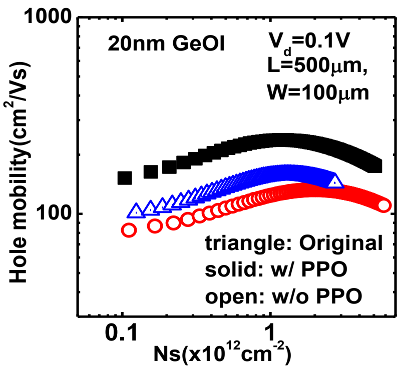

Fig.3: Effective hole mobility of 20nm GeOI with different back interface

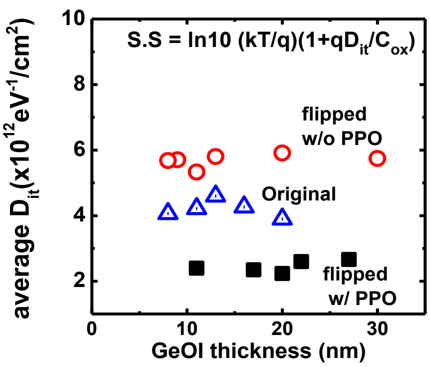

Fig.4: Thickness dependence of average D_{it} value of different back interface from S.S factors

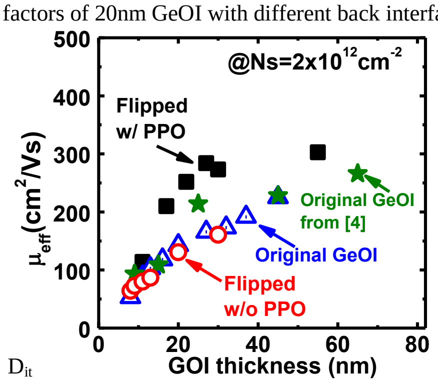

Fig.5: Thickness dependence of hole mobility