

Germanium for advanced CMOS transistors: Status and Trends

**J. Mitard, L. Witters, H. Arimura, Y. Sasaki, A.P. Milenin, R. Loo, A. Hikavy, G. Eneman,
P. Lagrain, H. Mertens, S. Sioncke, C. Vrancken, H. Bender, N. Horiguchi, A. Mocuta,
N. Collaert, A.V-Y. Thean
Imec, Kapeldreef 75, B-3001 Leuven, Belgium
E-mail: Jerome.Mitard@imec.be**

Over the past decades, germanium has gotten in the focal point of many research teams across the world aiming at replacing the 40+ -year-old silicon channel material used in CMOS technology. The main promise is the following: to contain and even reduce the power dissipation in ultra-scaled future technologies. Indeed, the threshold voltage (V_{TH}) of MOSFETs which is a measure of how much voltage is needed to initiate the channel conduction, cannot be strongly scaled down due to first, the “non-scaling” of the sub-threshold swing (with a minimum of 60 mV/decade at room temperature (300 K) for a “well-passivated” channel MOSFET) and secondly, due to the need of a low off-state leakage (stand-by energy consumption). Maintaining an high gate overdrive with respect to the power supply voltage (V_{DD}) will undeniably lead to a performance loss of Silicon-based circuits used in advanced portable electronic products for instance.

Boosting the device performance at lower V_{DD} is expected by the introduction of high mobility materials like SiGe [1], Ge [2], GeSn [3] or III/V [4] compound semiconductors. Moreover, in order to raise industry’s interest in these new devices, new channel materials have to be compatible with the regular FinFET-based technology and can be also integrated on a Silicon platform to reduce the time-to-market introduction and the associated cost.

In this work, we will investigate the “all-Ge” CMOS option namely a heterogeneous integration of strained Ge and relaxed SiGe for the PMOS and subsequently, a fully-relaxed Ge channel for the NMOS. The choice of these materials will first be justified by TCAD simulations. The integration challenges of both transistor types will be discussed with a specific focus on channel passivation, Source/Drain engineering and contact formation. Experimental data from our advanced test vehicle will be shown before drawing first conclusions about the strong and weak points of both Ge-based MOSFETs.

[1] J. Mitard et al., VLSI Technology, 2012 [2] J. Mitard, IEDM, 2008 [3] S. Gupta et al., Techn. Dig. IEDM, 978 (2012). [4] N. Waldron et al., Tech. Dig. VLSI Technol., 32 (2014).