

Three-terminal device for realizing a voltage-driven spin transistor

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Spin transistor is one of the attracted device due to additional functionalities, such as switching, amplification, and non-volatility. Recently, high power amplification of 130 has been demonstrated using current-field-driven spin transistor owing to the giant tunnel magnetoresistance (TMR) effect [1]. However this type of spin transistor exhibits lower performance as decreasing the size of the device. In this study, we proposed a new type of spin transistor, namely, voltage-driven spin transistor [2].

Fig. 1 (a) shows the concept of our proposed device. The magnetization of free layer can be controlled by applying a gate-to-source voltage via modulation of perpendicular magnetic anisotropy [3], which results in a resistance change in the MTJ due to TMR effect. If the change in output power is larger than the input power, the device can function as a spin transistor with power amplification.

Fig. 1 (b) shows the estimated power gain as functions of device width and resistance-area (RA) product for the thin-MgO layer. In the calculation, we assumed that the application of a gate voltage switches the magnetic easy axis of the free layer between the in-plane and out-of-plane direction. Higher power amplification can be expected as decreasing the device scale and RA value, and greater than 10^4 is achievable if we employ the three-terminal device with a junction size less than 50 nm, and RA value less than $5 \Omega \cdot \mu\text{m}^2$, as indicated by the shaded region in Fig. 1 (b). In the presentation, we also discuss the fabrication process of this type of spin transistor.

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[1] K. Konishi *et al.*, *IEEE Trans. Magn.* **48**, 1134 (2012)

[2] Y. Shiota *et al.*, submitted.

[3] T. Maruyama *et al.*, *Nat. Nanotechnol.* **4**, 158 (2009)

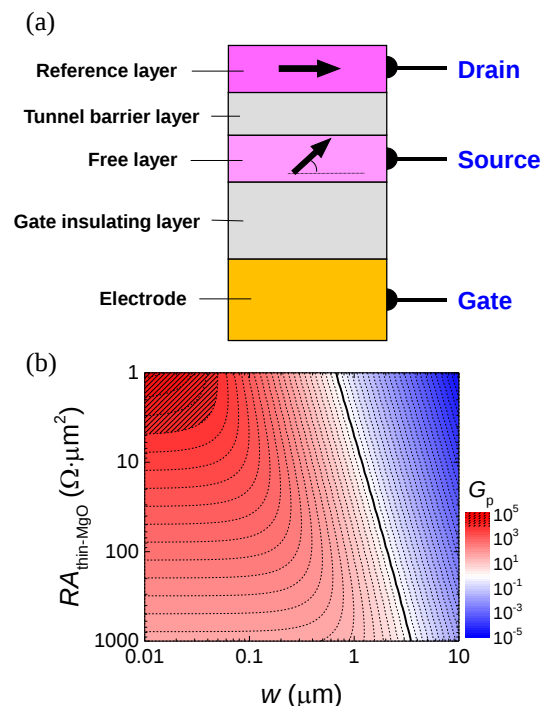


Figure 1 (a) Concept of the three-terminal device for realizing a voltage-driven spin transistor. (b) Theoretical calculation of power gain (G_p) according to device width (w) and resistance-area product for the thin-MgO layer ($RA_{\text{thin-MgO}}$)