

## Design Methodology for Very-Large-Scale-Integration of Adiabatic Quantum-Flux-Parametron Logic Superconductor Circuits

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Novel computing devices bring forth the need to re-evaluate and potentially develop new systematic methodologies that enable their large-scale integration of complex circuits and systems. Adiabatic quantum-flux-parametron (AQFP) logic is an emerging technology in superconducting electronics that shows promise towards building extremely energy efficient computing systems with bit energies approaching  $100k_B T$ . Circuits such as an 8-bit Kogge-Stone parallel prefix carry look-ahead adder consisting of more than 1,000 Josephson junctions have already been demonstrated. Additionally, the operation of quantum-flux-latches (QFLs), compatible with AQFP logic circuits as a basic memory element, has also been experimentally confirmed. To continue moving towards very-large-scale-integration (VLSI), it is necessary to carefully and systematically abstract the low-level physics from the logic-level design of VLSI AQFP systems. In this talk, we describe the development of an AQFP cell library (Fig. 1) as a collection logic building blocks used to construct a digital circuit. The cell library includes logic-level models (Fig. 2) using a combination of finite-state machines and transport delay parameters to simulate logic functionality and impact of long AC power-clock bias lines used to excite AQFP gates. Such an approach will provide invaluable design and simulation flows for developing more complex VLSI AQFP circuits and ensure their critical timing closure.

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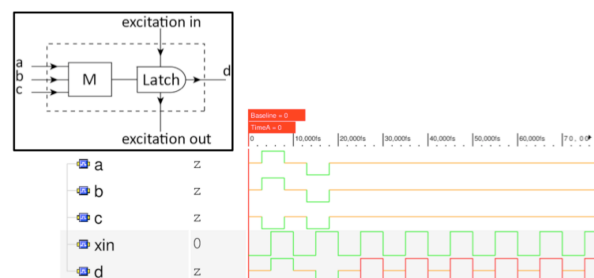
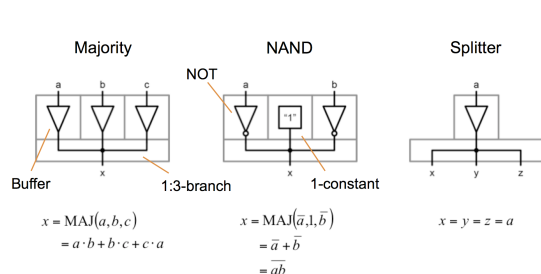


Fig. 1 Basic logic building blocks in the AQFP cell library.

Fig. 2 Conceptual diagram of logic modeling and corresponding waveform from logic simulation.