Effective reduction of parasitic resistance in Ge *p*-MOSFETs by ion implantation after germanidation technique

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Ge has been considered as a very promising channel material for replacing Si due to its higher carrier mobility than that of Si. Much improvement has been reported for Ge-based MOS devices over the past decade. However, it is still very challenging to achieve ultra-shallow junction as well as ultra-low parasitic resistance on Ge MOS devices. With an appropriate drive-in annealing, ion implantation after germanidation (IAG) technique has been considered an effective way to form ultra-shallow junction without Fermi level pinning (FLP) at metal/Ge interface.[1,2] To investigate the impact on device performances by IAG technique, in this work, Ge *p*-MOSFETs with self-aligned metallic NiGe S/D formed by IAG technique were fabricated. With increasing drive-in annealing temperature, effective reduction in parasitic resistance (R_{para}) of Ge *p*-MOSFET was demonstrated.[3]

The relationship between measured resistivity (R_m) and effective gate length (L_{eff}) for varying gate overdrive values of Ge *p*-MOSFETs fabricated with and without IAG technique is shown in Fig. 1 (a) and (b). R_{para} reduced about five times for the devices fabricated with IAG technique and low R_{para} of 835 Ω-μm was achieved on Ge *p*-MOSFETs after 450 °C drive-in annealing. The components in R_{para} for the Ge *p*-MOSFETs have been analyzed and summarized in Fig. 2. The reduction of R_{para} is actually by means of the decrease for both sheet resistance (R_s) and spreading resistance (R_{sp}). It is noted that high temperature annealing has benefits in IAG technique, which helps to decrease the R_{para} in Ge *p*-MOSFETs while the thermal stability of the whole gate stack has to be considered for achieving high mobility channel as well as low R_{para}.

In conclusion, we demonstrate the effect of IAG technique in the device performance of Ge *p*-MOSFETs with the low R_{para} of 835 Ω-μm. The results can be readily applied to future Ge *p*-MOSFETs for achieving shallow junction and low parasitic resistance.

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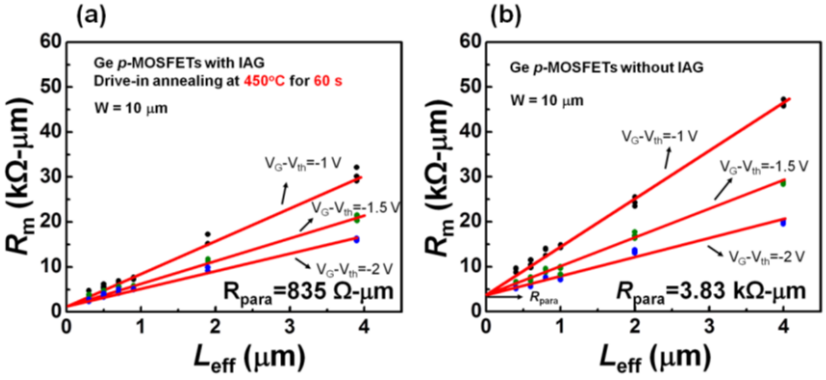

Fig. 1 Device measured resistivity (R_m) versus effective gate length (L_{eff}) at varying gate overdrives for Ge *p*-MOSFETs fabricated (a) with and (b) without IAG technique. The line intersects at one point gives the value to parasitic resistance (R_{para}).

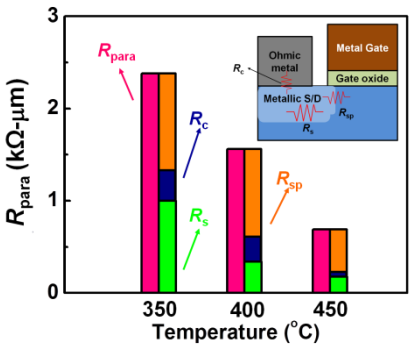

Fig. 2 Summary of R_{para}, R_s, contact resistance (R_c) and R_{sp} for Ge *p*-MOSFETs fabricated by IAG technique with different drive-in annealing temperatures. The inset shows the simple schematic diagram for a self-aligned metallic S/D MOSFET, with R_c, R_s and R_{sp} indicated.