Effects of strain, interface states and back bias on electrical characteristics of Ge-source UTB strained-SOI tunnel FETs

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1. Introduction Development of the optimum materials, structures and processing for TFET channel and source regions is of paramount importance for realizing both low subthreshold swing (*SS*) of sub-60 mV/dec and high drain on-current/off-current ratio (I_{on}/I_{off}) at the same time. As for the TFET channels, strained-Si (sSi) is a realistic material. Tensile strain TFETs with SiGe sources [1, 2] or nano-wire structures [3, 4] have already been reported. However, a systematic study of the impact of channel strain on TFET performance has not been performed yet. As for the TFET sources, pure Ge sources grown on Si are expected to provide higher tunneling current, because of the type-II staggered band alignment between Ge and Si [5], meaning that the strained Si TFETs with the pure Ge sources is promising [6]. However, the electrical characteristics of strained-Si TFETs combined with the Ge sources have not been fully studied yet. In this study, the impacts of tensile strain, interface states and back biasing on the electrical properties of the strained SOI TFETs with the Ge sources are systematically examined.

2. Experimental Results and Discussion Fig. 1 shows the schematic process flow of the present Ge/sSOI TFETs [8]. In-situ B-doped Ge, directly grown on SOI substrates, is used as the source region of TFETs. Fig. 2 shows the drain current-gate voltage (I_D-V_G) characteristics of the fabricated devices. It is found that an increase in strain leads to the increase in I_{on} and *SS* improvement. Fig. 3 and Fig. 4 show the I_{on}/I_{off} ratio and minimum *SS* (SS_{min}), respectively, as a function of PMA temperature. After 400 °C PMA, enhanced electrical characteristics with the I_{on}/I_{off} ratio of 7.9×10^6, 2.2×10^7 and 3.7×10^7 and SS_{min} of 69, 44 and 29 mV/dec are obtained for the unstrained, 0.8 and 1.1 % strained SOI TFETs, respectively. The better performance of TFETs with higher PMA temperature is attributed to more sensitive modulation of the surface potential of the Si channels with respect to V_G by reduction in D_{it} after PMA [7]. Fig. 5 shows the back bias (V_B) dependencies of *SS* and I_{on}/I_{off}. Negative V_B causes lower I_{off} resulting in lower SS_{min}. On the other hand, positive V_B yields the significant increase in I_{on} and the decrease in *SS* in a wide range of middle I_D region, in spite of the increase in I_{off} due to the increase in the ambipolar current. As a result, the V_B control can be an effective way to improve the performance of SOI-based TFETs.

3. Conclusions The electrical characteristics of Ge/strained-Si hetero-junction TFETs with in-situ B-doped Ge have been studied. It has been found that higher strain in the channel, the optimized PMA process, and the positive back biasing can enhance the electrical properties.

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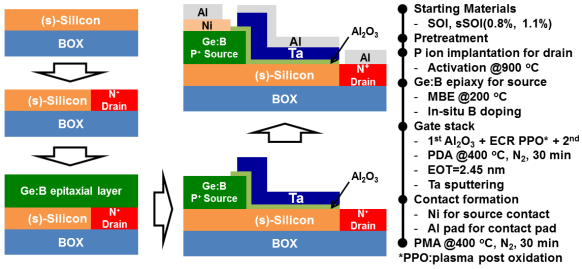

Fig. 1 Process flow of the proposed devices.

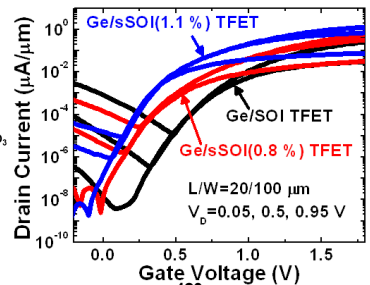

Fig. 2 I_D-V_G characteristics of the fabricated devices.

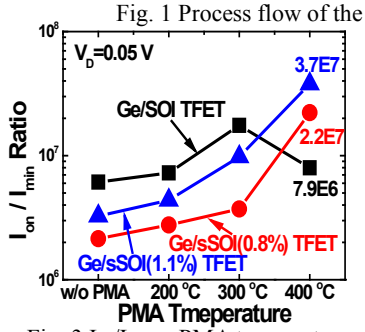

Fig. 3 I_{on}/I_{off} vs PMA temperature

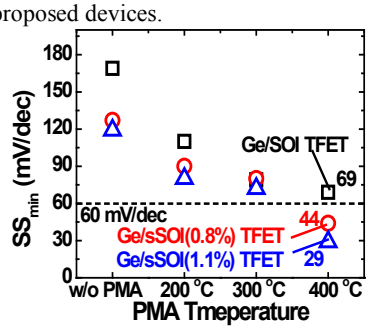

Fig. 4 SS_{min} vs PMA temperature

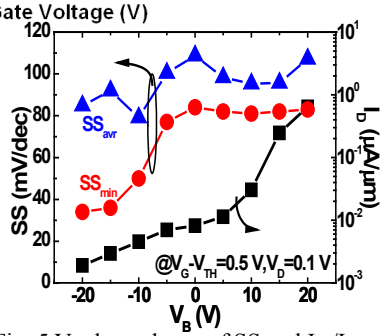

Fig. 5 V_B dependence of SS and I_{on}/I_{off}