Planar Device Isolation for β-Ga_2O_3 Field Effect Transistors

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Mesa-free inter-device electrical isolation on a chip, typically achieved through ion implantation damage of conductive epitaxial layers, is desirable for improving manufacturing yield and process uniformity by preserving wafer planarity as well as eliminating mesa sidewall leakage. Ga_2O_3 – a strong contender for the next-generation power devices due to its wide 4.8-eV bandgap and the availability of economical native substrates – benefits uniquely from the high flexibility offered by Si ion (Si^+) implantation doping in device placement on unintentionally-doped (UID) material [1]. This work demonstrates that UID Ga_2O_3 grown by molecular beam epitaxy (MBE) is highly resistive and can be adopted for effective planar isolation of Ga_2O_3 devices formed by selective-area Si^+ implantation doping of the UID epilayer.

Three UID Ga_2O_3 epilayers with respective thicknesses of 0.5 µm, 1.0 µm, and 1.5 µm were grown by ozone MBE on Fe-doped β-Ga_2O_3 (010) substrates. Isolation test structures, consisting of two 110-µm-wide conductive regions spaced 10 – 80 µm apart, were fabricated by selective-area Si^+ implantation doping and Ti/Au Ohmic metallization [2]. Leakage currents measured at 200-V bias across the 10-µm gap spacing were typically less than 0.2 nA/mm. Destructive breakdown voltages, being limited by electric field concentration around sharp corners, could exceed 1000 V (Fig. 1). The temperature-dependent conductance ($\sigma(T)$) did not scale with the thickness of the UID buffer, which was a strong indication of surface and/or sub-surface leakage instead of bulk conduction. Furthermore, a plot of $\ln(\sigma(T))$ against $1/T$ did not follow an Arrhenius linear relationship. It was thereby shown that the leakage followed 2-D variable-range hopping transport as described by $\sigma(T) \propto \exp[-(T_0/T)^{1/(d+1)}]$, where T_0 is a characteristic temperature and d = 2 is the dimension of the system (Fig. 2) [3]. Hopping conduction was consistent with the disordered nature of a surface, where carrier transport was facilitated by surface states. With proper surface passivation, the highly-resistive UID Ga_2O_3 epilayer is viable for inter-device electrical isolation without mesa etching or ion damage.

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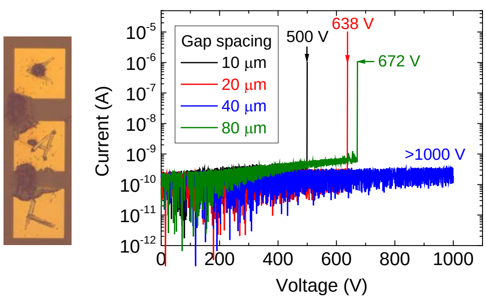

Fig. 1. Destructive breakdown voltages of 1.5-µm-thick UID Ga_2O_3 measured across various contact spacings. Failure occurred around sharp corners where electric field concentrated.

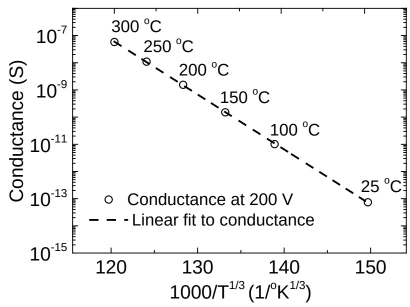

Fig. 2. Plot of $\ln(\sigma)$ against $1/T^{1/3}$ for 1.5-µm-thick epilayer at 200-V bias. A linear fit to the data indicated 2-D variable-range hopping transport.