AC performance improvement by RMG module for 14nm FinFETs and beyond

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Abstract
An advanced Replacement Metal Gate (RMG) module was developed for 14nm node FinFETs and beyond. Extra STI oxide recess increases on-current without any dedicated Source and Drain (SD) optimization. Selective Tungsten (W) etch recesses work function metal (WFM), which reduces gate-contact capacitance, and improves AC performance and yields by increasing gate-contact space.

Introduction
FinFET is becoming the de-facto standard logic device for the 14nm node and beyond [1, 2]. It is essential for AC performance to minimize parasitic resistance and parasitic capacitance. SD engineering is the most popular technique to improve DC performance [3, 4]. In this work, we focus on optimizations in the RMG module to improve AC performance [5].

Experiments
The FinFET devices were built with a dummy gate on a 14nm node design rule (Fig. 1 (a)). In the RMG module, an additional STI oxide etch step was introduced after dummy gate removal, which increases the effective fin height (Fig. 1 (b)). After WFM fill, W gates were recessed for self-aligned contacts (Fig. 1 (d) and (e)). In our work, W was selectively etched to create space for the gate-contact (Fig. 1 (d)).

Results and Discussions
A. Extra STI oxide recess for high on-current
Figure 2 shows TEM pictures of the extra STI oxide etch. STI oxide recess makes fin bottom deeper only under the gate and increases the effective fin height that results in the channel width increase and thereby on-current increase of the device (Fig. 2 (a) and (b)). The fin of the SD area is not changed (Fig. 2 (c) and (d)). Thus effective fin height increase can be achieved without significant addition to the integration and sacrificing short channel effects (SCE).

B. Selective W etch for low parasitic capacitance
Figure 3 (a) shows the gate structure after standard W recess at RMG. Selective W etch makes the gate height difference between WFM and W as shown in Fig. 3 (b) and (c), and creates space of the gate-contact (Fig. 3 (d)). Gate-contact short yield is improved by extended selective W etch without adversely impacting on the gate sheet resistance. From device performance point of view, selective W etch reduces the gate-contact parasitic capacitance and improves AC performance.

Conclusions
We developed the advanced RMG module for 14nm node FinFETs and beyond, which improves on-current, AC performance, and yield. Extra STI oxide recess during RMG module increases on-current without dedicated process like SD optimization. Selective W etch improves AC performance and gate-contact short yield.

References