AC performance improvement by RMG module for 14nm FinFETs and beyond

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Abstract

An advanced Replacement Metal Gate (RMG) module was developed for 14nm node FinFETs and beyond. Extra STI oxide recess increases on-current without any dedicated Source and Drain (SD) optimization. Selective Tungsten (W) etch recesses work function metal (WFM), which reduces gate-contact capacitance, and improves AC performance and yields by increasing gate-contact space.

Introduction

FinFET is becoming the de-facto standard logic device for the 14nm node and beyond [1, 2]. It is essential for AC performance to minimize parasitic resistance and parasitic capacitance. SD engineering is the most popular technique to improve DC performance [3, 4]. In this work, we focus on optimizations in the RMG module to improve AC performance [5].

Experiments

The FinFET devices were built with a dummy gate on a 14nm node design rule (Fig. 1 (a)). In the RMG module, an additional STI oxide etch step was introduced after dummy gate removal, which increases the effective fin height (Fig. 1 (b)). After WFM fill, W gates were recessed for self-aligned contacts (Fig. 1 (d) and (e)). In our work, W was selectively etched to create space for the gate-contact (Fig. 1 (d)).

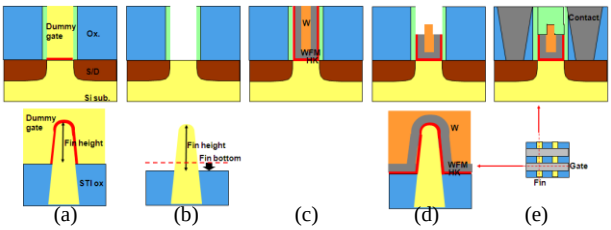

Fig. 1 Advanced RMG module on 14nm node design rule. Top is x-section across gate, bottom is across fin. (a) Before dummy gate removal. (b) After dummy gate removal. Extra STI oxide recess is performed for higher on-current. (c) WFM/W fill. (d) Selective W etch to reduce parasitic capacitance keeping low gate resistance. (e) Contact formation with SAC.

Results and Discussions

A. Extra STI oxide recess for high on-current

Figure 2 shows TEM pictures of the extra STI oxide etch. STI oxide recess makes fin bottom deeper only under the gate and increases the effective fin height that results in the channel width increase and thereby on-current increase of the device (Fig. 2 (a) and (b)). The fin of the SD area is not changed (Fig. 2 (c) and (d)). Thus effective fin height increase can be achieved without significant addition to the integration and sacrificing short channel effects (SCE).

B. Selective W etch for low parasitic capacitance

Figure 3 (a) shows the gate structure after standard W recess at RMG. Selective W etch makes the gate height difference between WFM and W as shown in Fig. 3 (b) and (c), and creates space of the gate-contact (Fig. 3 (d)). Gate-contact short yield is improved by extended selective W etch without adversely impacting on the gate sheet resistance. From device performance point of view, selective W etch reduces the gate-contact parasitic capacitance and improves AC performance.

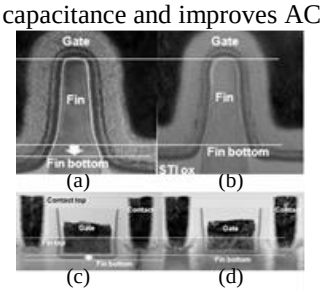

Fig. 2 Fin with extra STI oxide recess (a) and w/o extra recess (b) on XTEM images across fin. (c) and (d) are XTEM images across gate w/ and w/o extra STI oxide recess respectively.

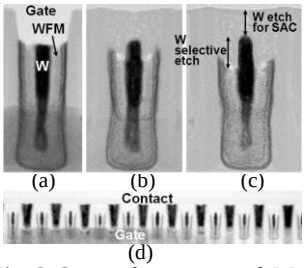

Fig. 3 Gate with conventional W etch (a), selective W etch (b), longer selective W etch (c). (d) FinFET across gate with selective W etch.

RO delay vs. RO effective switching capacitance (Ceff [6]) for various combinations of extra STI oxide etch and selective W etch processes are shown in Fig. 4. The delay-Ceff plot can be used as a metric to optimize/gauge the RO performance improvement using process parameters under study. Selective W etch reduces Ceff and decreases RO delay on the same (IDDA-IDDQ) trend line. On the other hand, effective taller fins from extra STI oxide recess increases IDDA-IDDQ and decreases RO delay. The intersection of the family of fixed IDDA-IDDQ lines shows intrinsic capacitance without any gate related parasitics. These results indicate the optimal combination of selective W etch for shorter gate and extra STI oxide recess for taller fin improves AC performance.

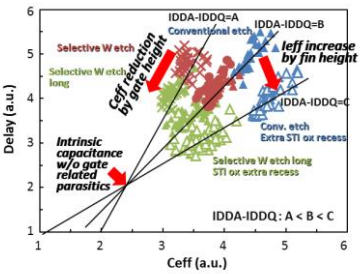

Fig. 4 RO delay and Ceff with extra STI oxide recess and selective W etch as a function of IDDA-IDDQ.

Conclusions

We developed the advanced RMG module for 14nm node FinFETs and beyond, which improves on-current, AC performance, and yield. Extra STI oxide recess during RMG module increases on-current without dedicated process like SD optimization. Selective W etch improves AC performance and gate-contact short yield.

References

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